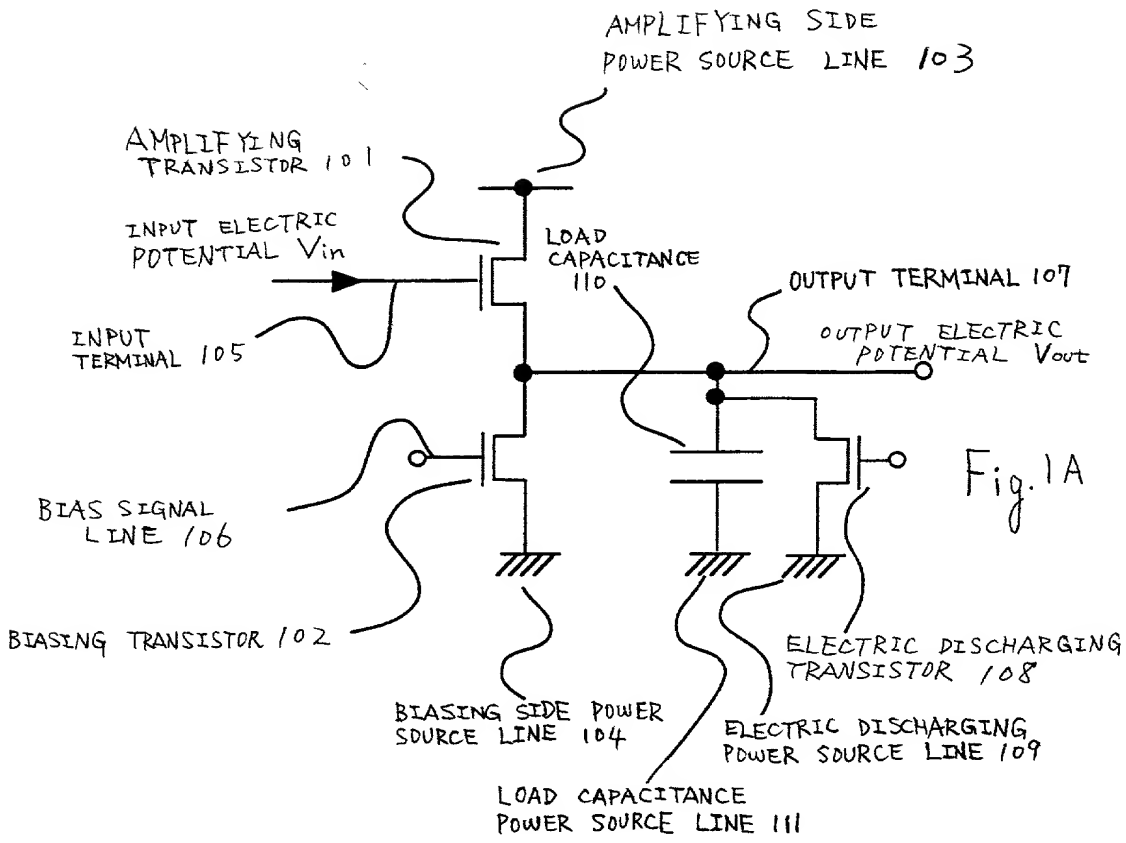

AMPLIFYING SIDE POWER SOURCE LINE 103
AMPLIFYING TRANSISTOR 101
INPUT ELECTRIC POTENTIAL Vin
LOAD CAPACITANCE 110
OUTPUT TERMINAL 107
INPUT TERMINAL 105
OUTPUT ELECTRIC POTENTIAL Vout
BIAS SIGNAL LINE 106
BIASING TRANSISTOR 102
ELECTRIC DISCHARGING TRANSISTOR 108
BIASING SIDE POWER SOURCE LINE 104
ELECTRIC DISCHARGING POWER SOURCE LINE 109
LOAD CAPACITANCE POWER SOURCE LINE 111

Fig. 1A

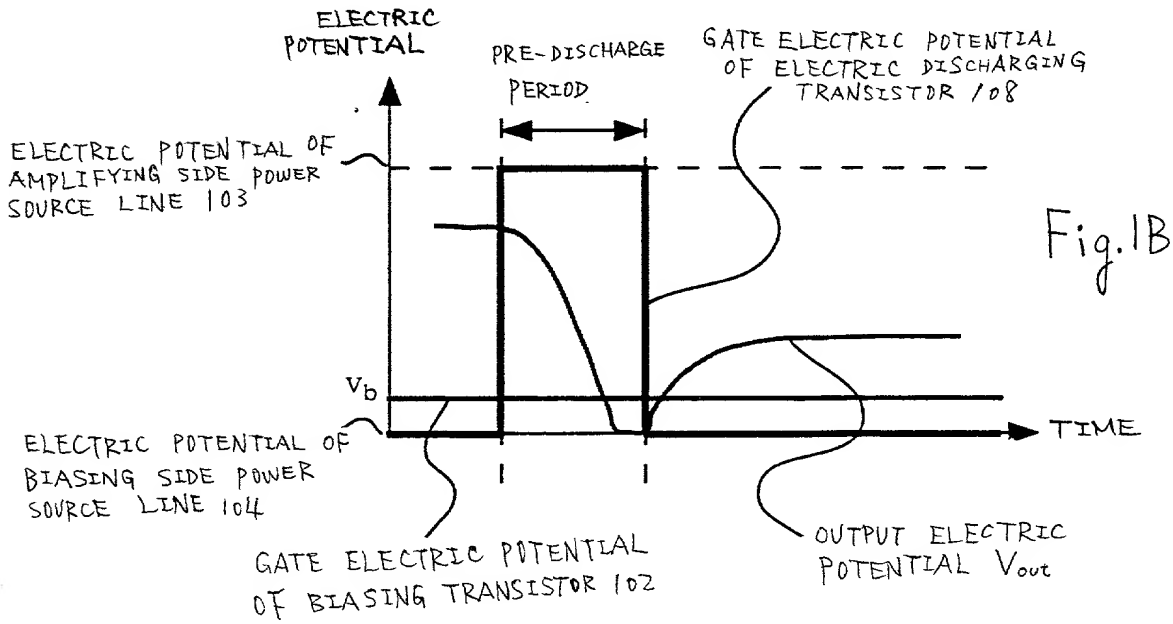
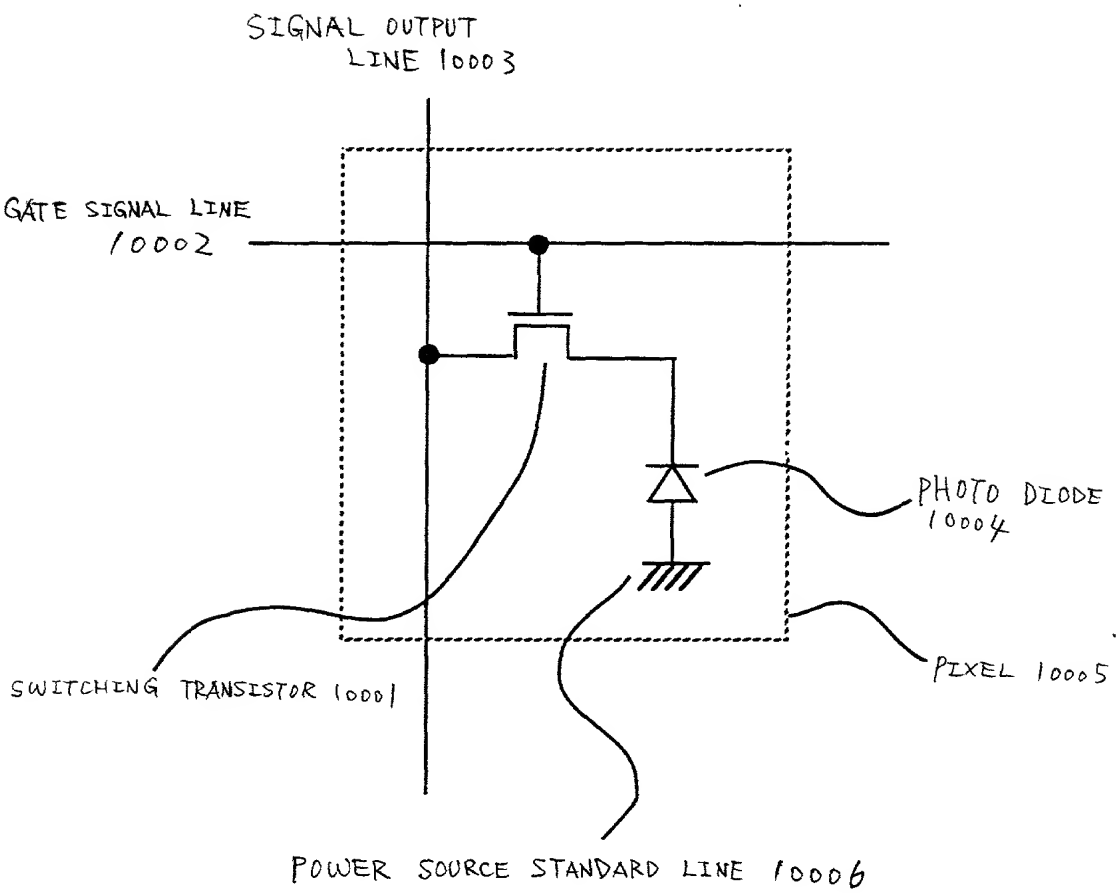

ELECTRIC POTENTIAL
PRE-DISCHARGE PERIOD
GATE ELECTRIC POTENTIAL OF ELECTRIC DISCHARGING TRANSISTOR 108
ELECTRIC POTENTIAL OF AMPLIFYING SIDE POWER SOURCE LINE 103
Vb
TIME
ELECTRIC POTENTIAL OF BIASING SIDE POWER SOURCE LINE 104
GATE ELECTRIC POTENTIAL OF BIASING TRANSISTOR 102
OUTPUT ELECTRIC POTENTIAL Vout

Fig. 1B

Fig. 2


SIGNAL OUTPUT
LINE 10003
GATE SIGNAL LINE
10002
PHOTO DIODE
10004
PIXEL 10005
SWITCHING TRANSISTOR 10001
POWER SOURCE STANDARD LINE 10006

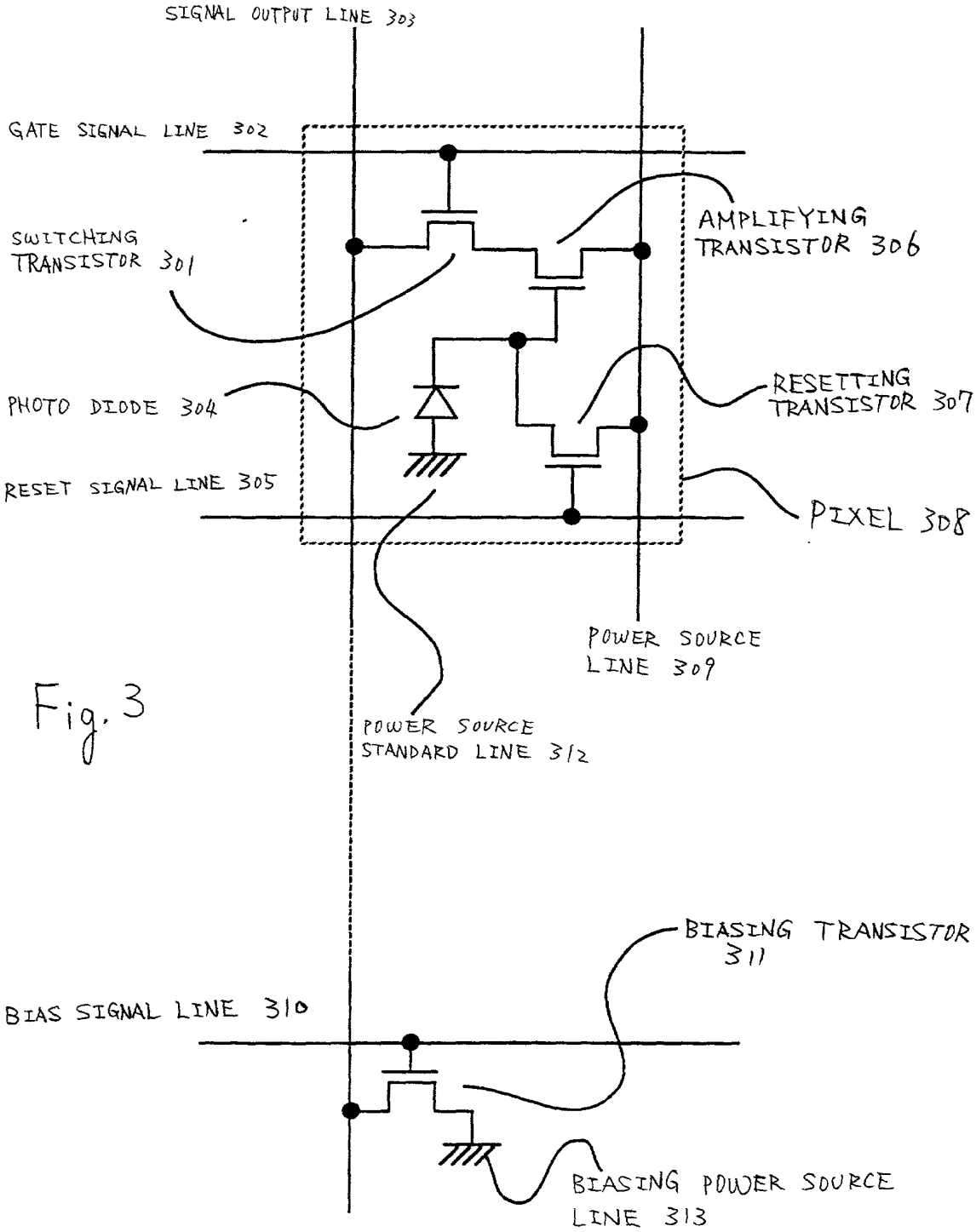

SIGNAL OUTPUT LINE 303
GATE SIGNAL LINE 302
SWITCHING TRANSISTOR 301
AMPLIFYING TRANSISTOR 306
PHOTO DIODE 304
RESETTING TRANSISTOR 307
RESET SIGNAL LINE 305
PIXEL 308
POWER SOURCE LINE 309
POWER SOURCE STANDARD LINE 312
BIASING TRANSISTOR 311
BIAS SIGNAL LINE 310
BIASING POWER SOURCE LINE 313

Fig. 3

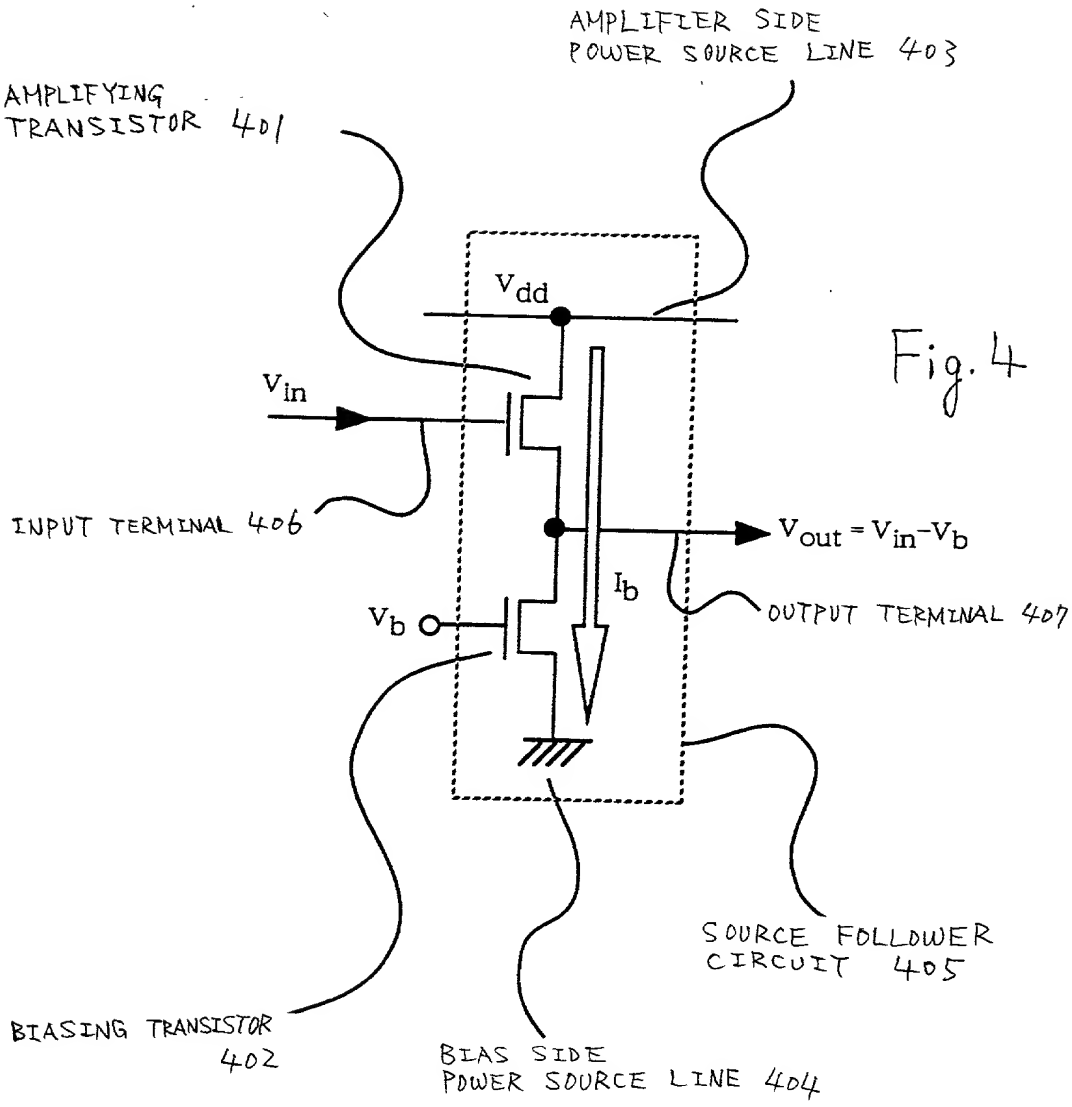

AMPLIFIER SIDE
POWER SOURCE LINE 403
AMPLIFYING
TRANSISTOR 401
V_{dd}
V_{in}
INPUT TERMINAL 406
$V_{out} = V_{in} - V_b$
I_b
V_b
OUTPUT TERMINAL 407
SOURCE FOLLOWER
CIRCUIT 405
BIASING TRANSISTOR
402
BIAS SIDE
POWER SOURCE LINE 404

Fig. 4

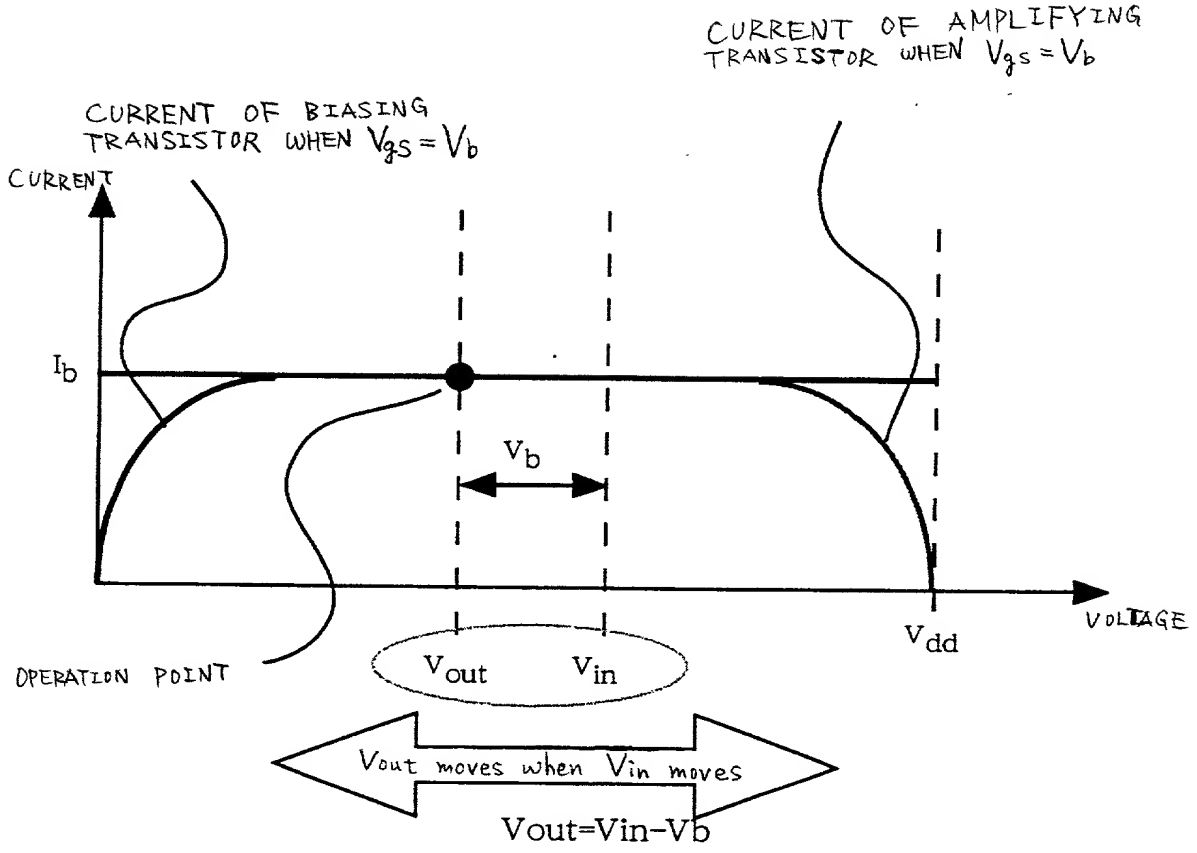

CURRENT OF AMPLIFYING TRANSISTOR WHEN $V_{gs} = V_b$
CURRENT OF BIASING TRANSISTOR WHEN $V_{gs} = V_b$
CURRENT
I_b
V_b
VOLTAGE
V_{dd}
OPERATION POINT
V_{out}
V_{in}
Vout moves when Vin moves
Vout=Vin-Vb

Fig. 5

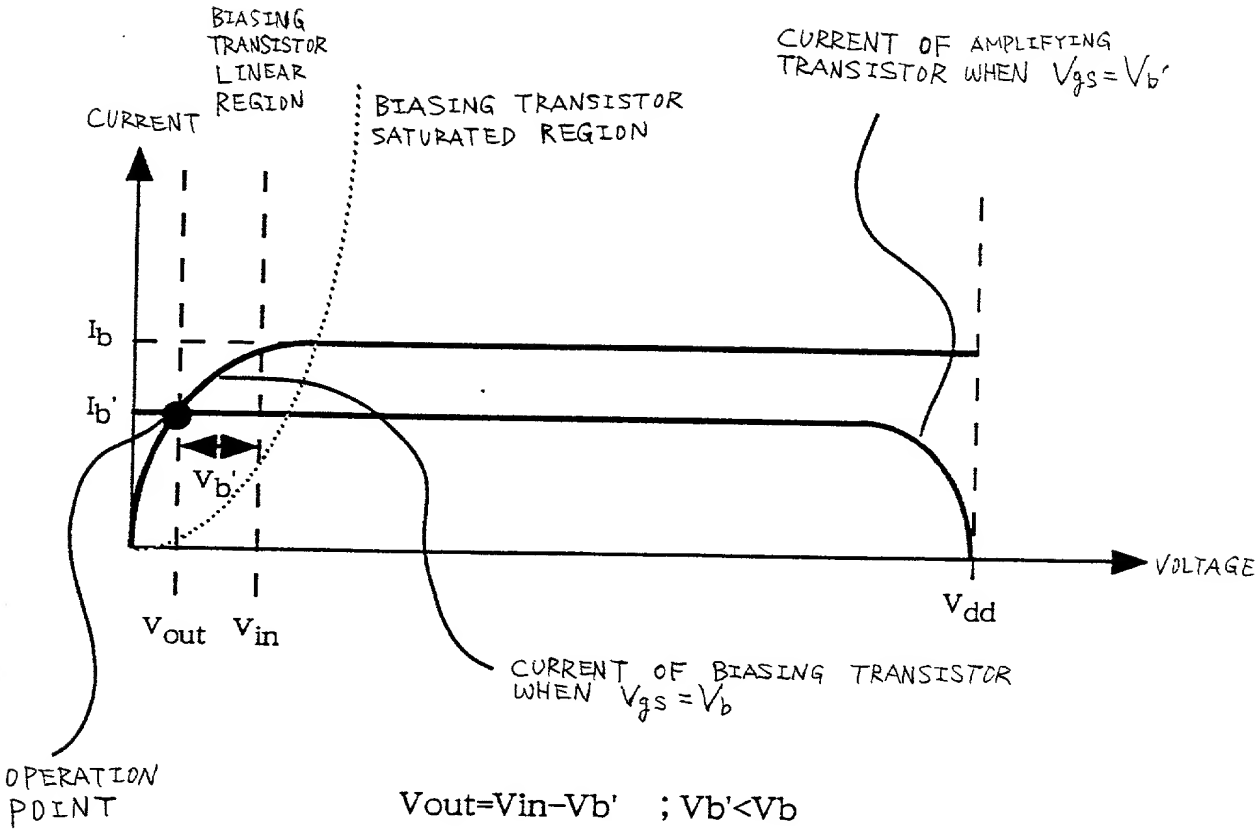

BIASING TRANSISTOR LINEAR REGION
BIASING TRANSISTOR SATURATED REGION
CURRENT OF AMPLIFYING TRANSISTOR WHEN $V_{gs}=V_b'$
CURRENT
I_b
I_b'
V_b'
VOLTAGE
V_{out}
V_{in}
V_{dd}
CURRENT OF BIASING TRANSISTOR WHEN $V_{gs}=V_b$
OPERATION POINT
$V_{out}=V_{in}-V_b'$; $V_b'<V_b$

Fig. 6

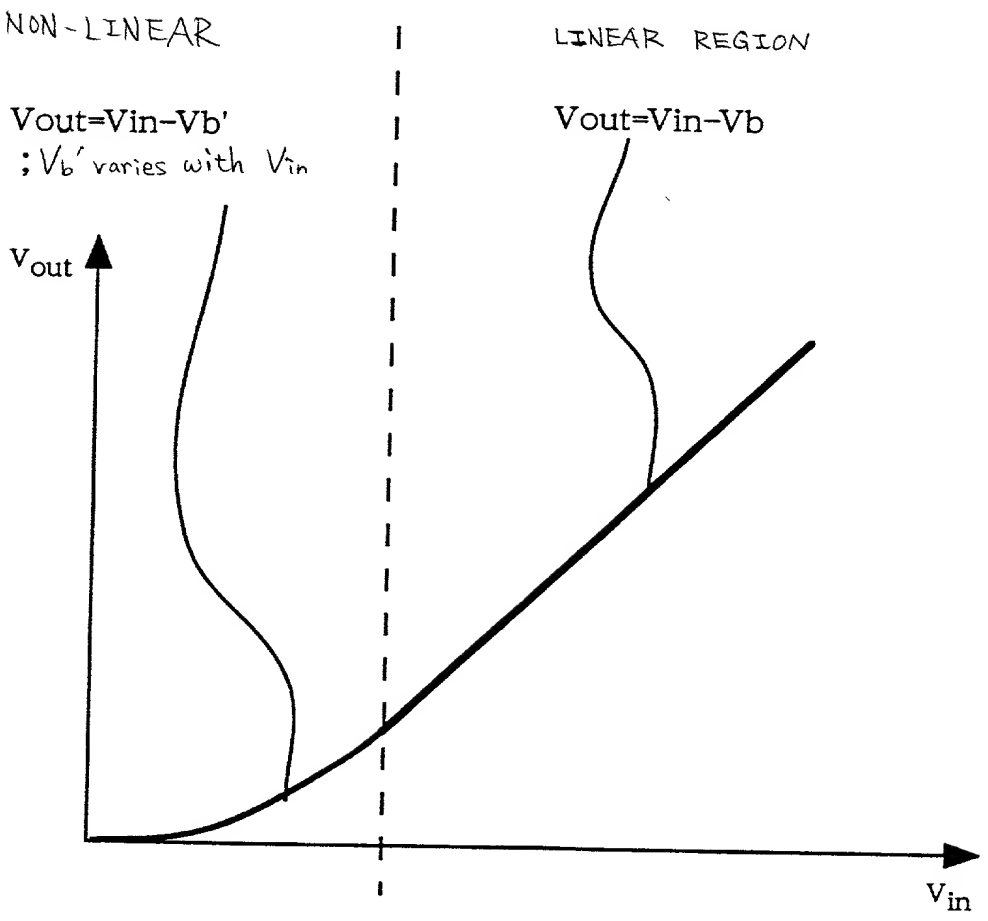

NON-LINEAR
LINEAR REGION
Vout=Vin-Vb'
; Vb' varies with Vin
Vout=Vin-Vb
Vout
Vin

Fig. 7

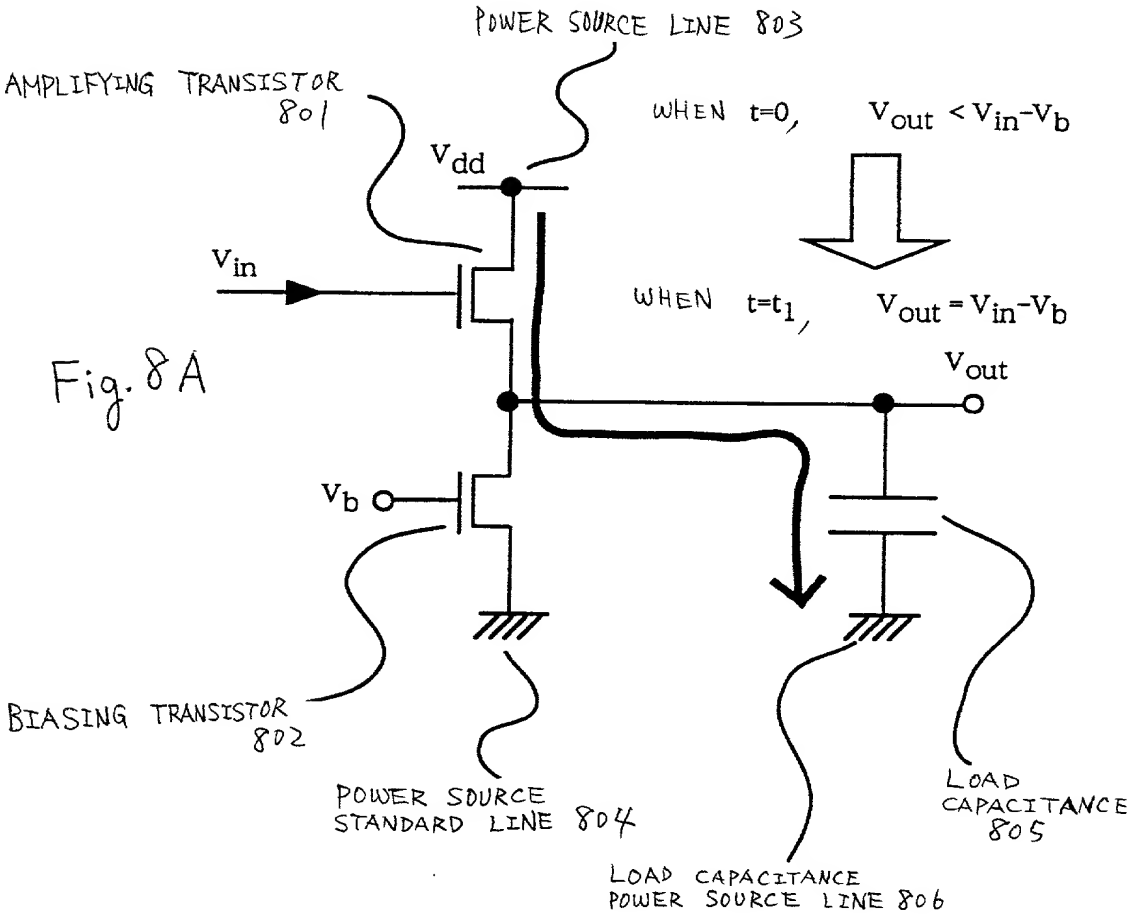

POWER SOURCE LINE 803
AMPLIFYING TRANSISTOR 801
V_{dd}
V_{in}
WHEN t=0, $V_{out} < V_{in}-V_b$
WHEN $t=t_1$, $V_{out} = V_{in}-V_b$
V_{out}
V_b
BIASING TRANSISTOR 802
POWER SOURCE STANDARD LINE 804
LOAD CAPACITANCE 805
LOAD CAPACITANCE POWER SOURCE LINE 806

Fig. 8A

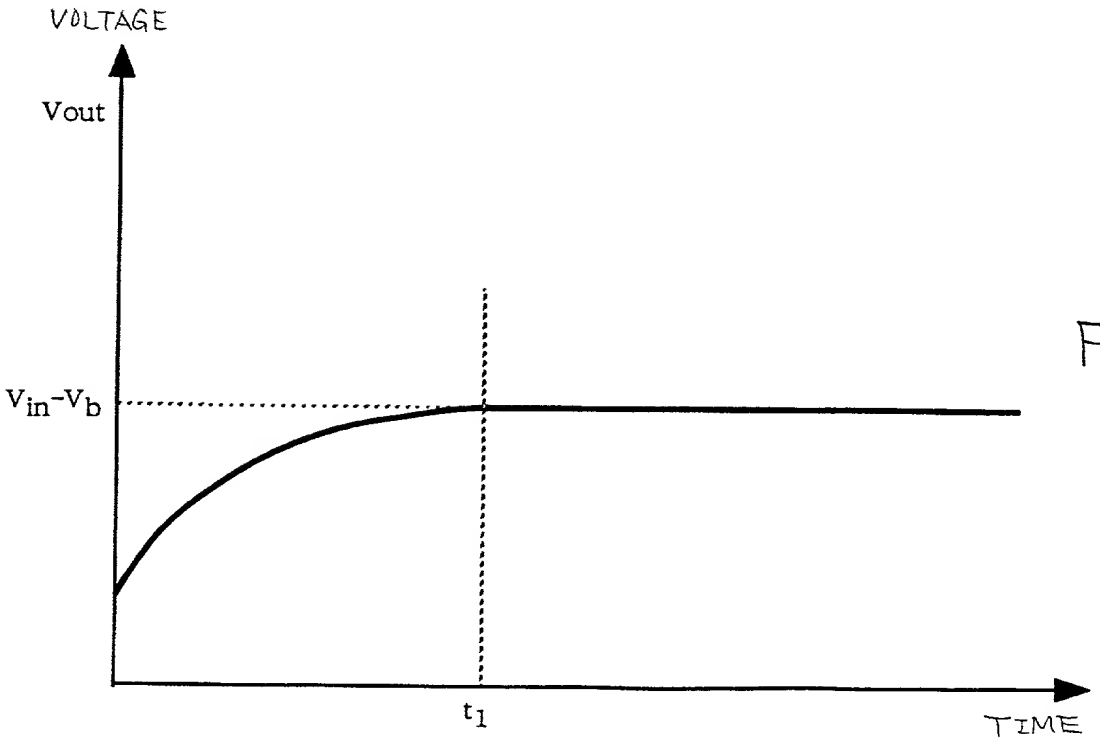

VOLTAGE
Vout
$V_{in}-V_b$
t_1
TIME t

Fig. 8B

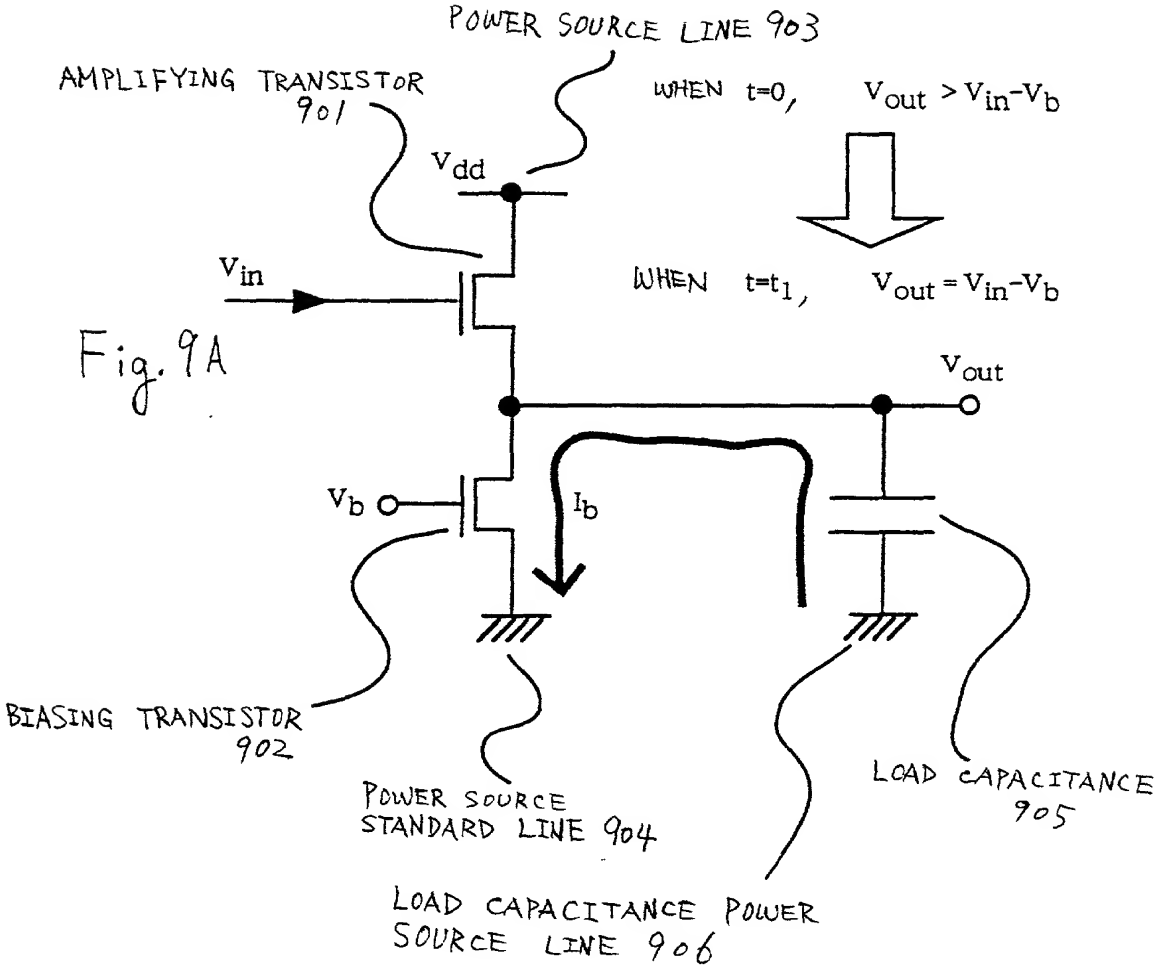

POWER SOURCE LINE 903
AMPLIFYING TRANSISTOR 901
WHEN t=0, Vout > Vin-Vb
Vdd
Vin
WHEN t=t1, Vout = Vin-Vb
Vout
Vb
Ib
BIASING TRANSISTOR 902
POWER SOURCE STANDARD LINE 904
LOAD CAPACITANCE 905
LOAD CAPACITANCE POWER SOURCE LINE 906

Fig. 9A

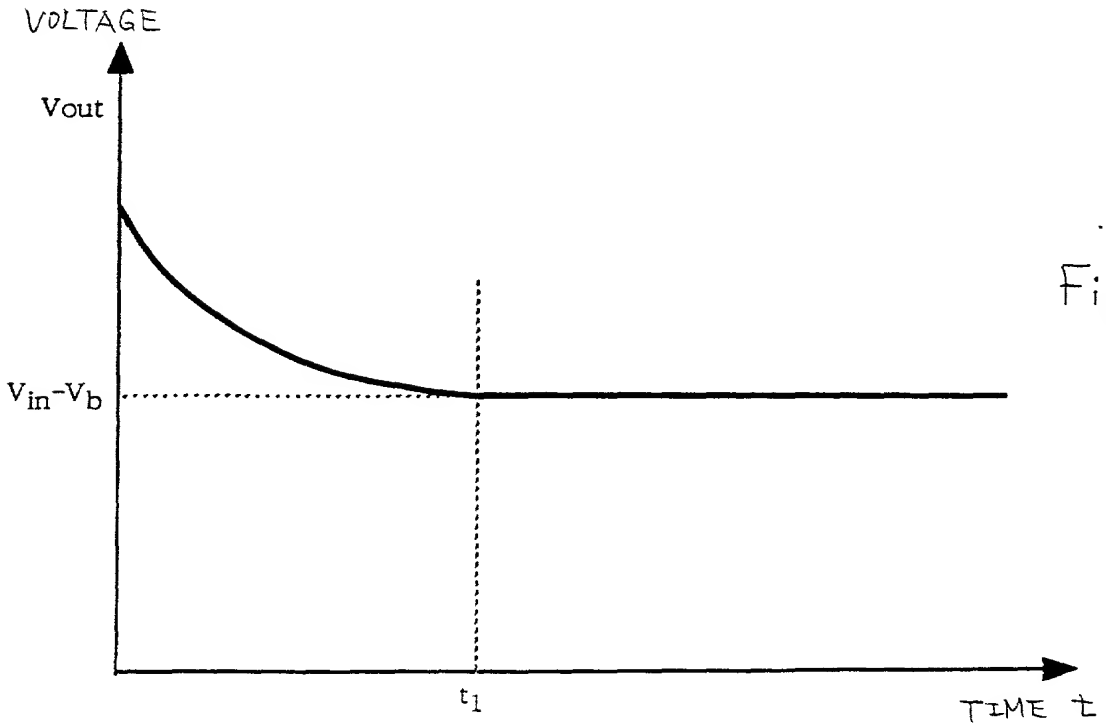

VOLTAGE
Vout
Vin-Vb
t1
TIME t

Fig. 9B

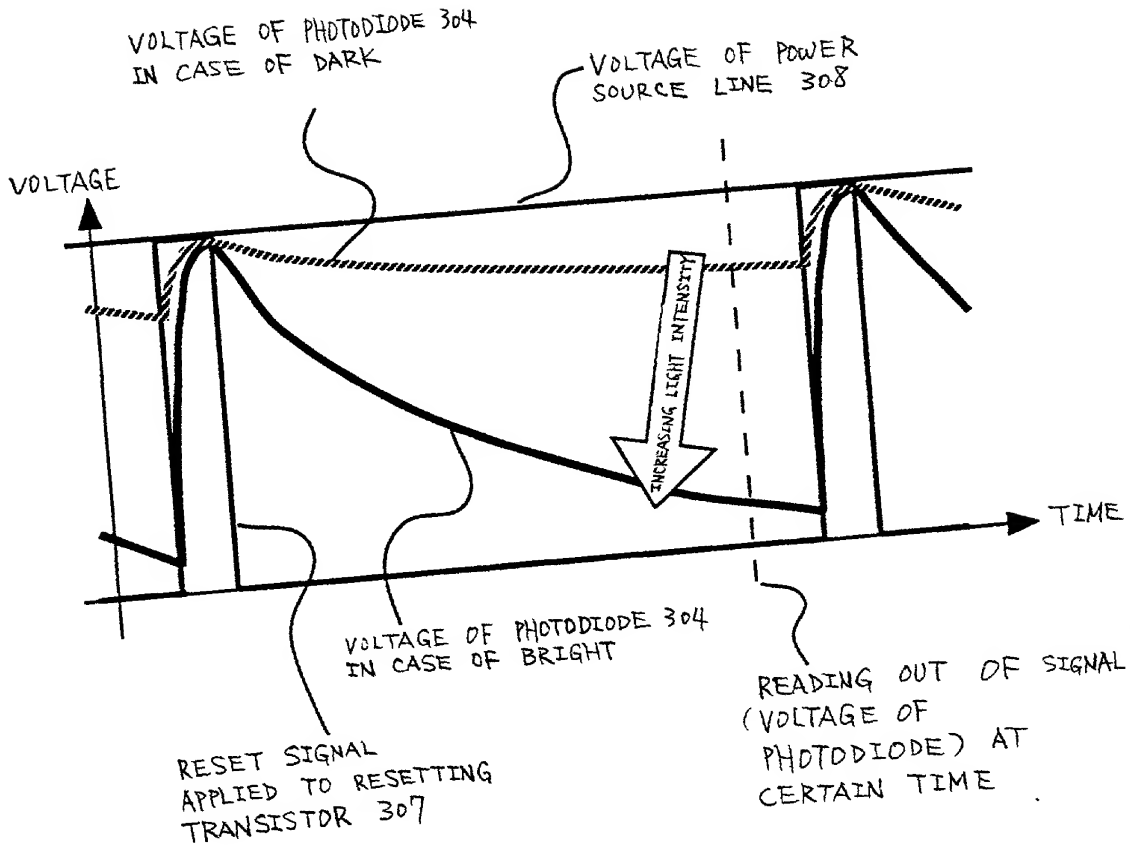

VOLTAGE OF PHOTODIODE 304
IN CASE OF DARK
VOLTAGE OF POWER
SOURCE LINE 308
VOLTAGE
INCREASING LIGHT INTENSITY
TIME
VOLTAGE OF PHOTODIODE 304
IN CASE OF BRIGHT
READING OUT OF SIGNAL
(VOLTAGE OF
PHOTODIODE) AT
CERTAIN TIME
RESET SIGNAL
APPLIED TO RESETTING
TRANSISTOR 307

Fig. 10

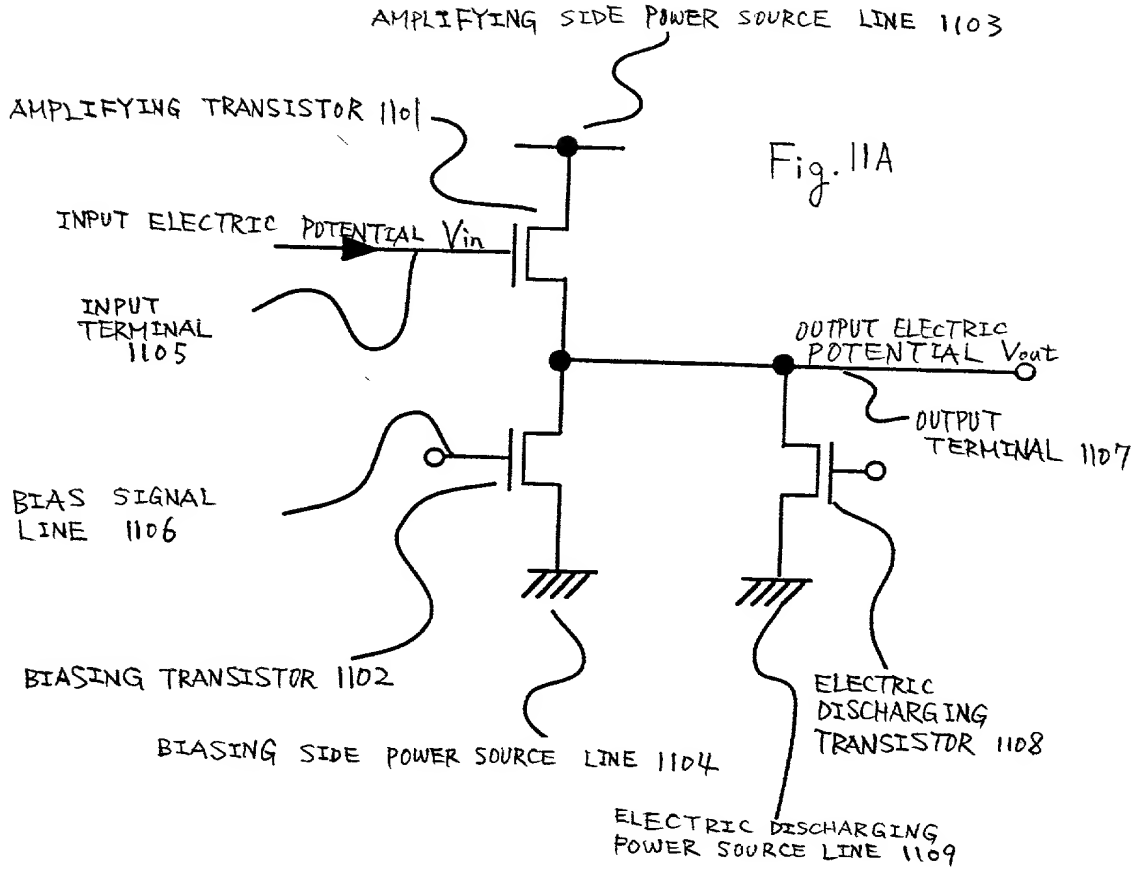


Fig. 11A

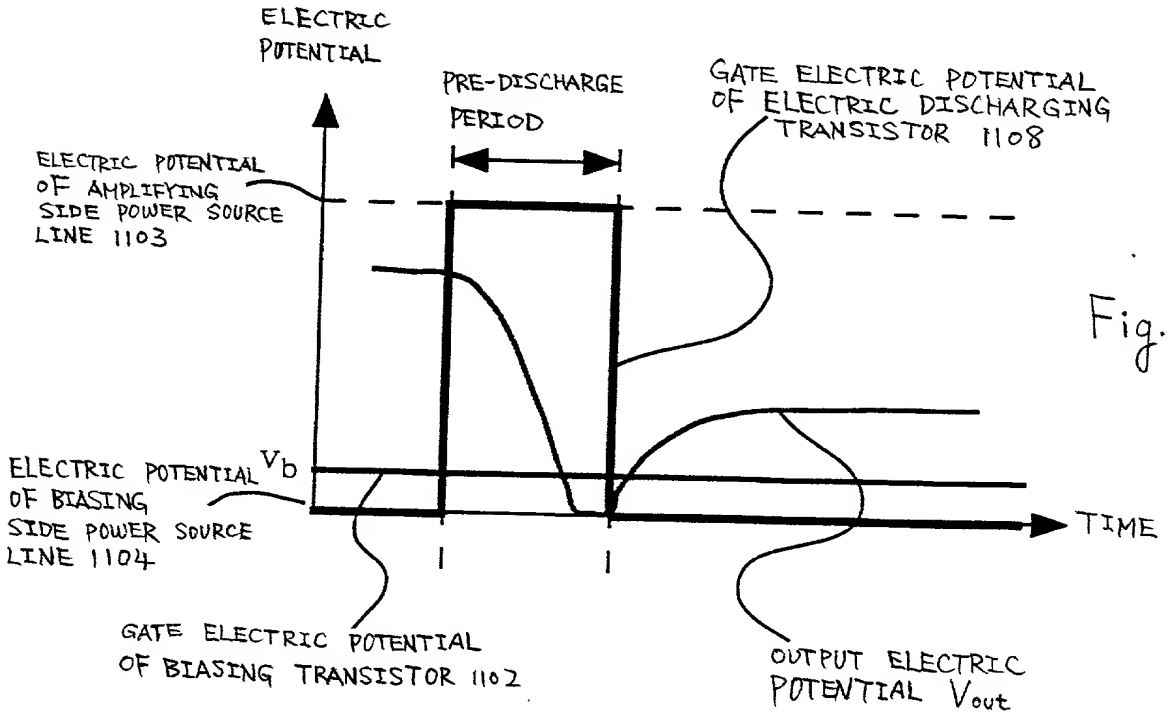


Fig. 11B

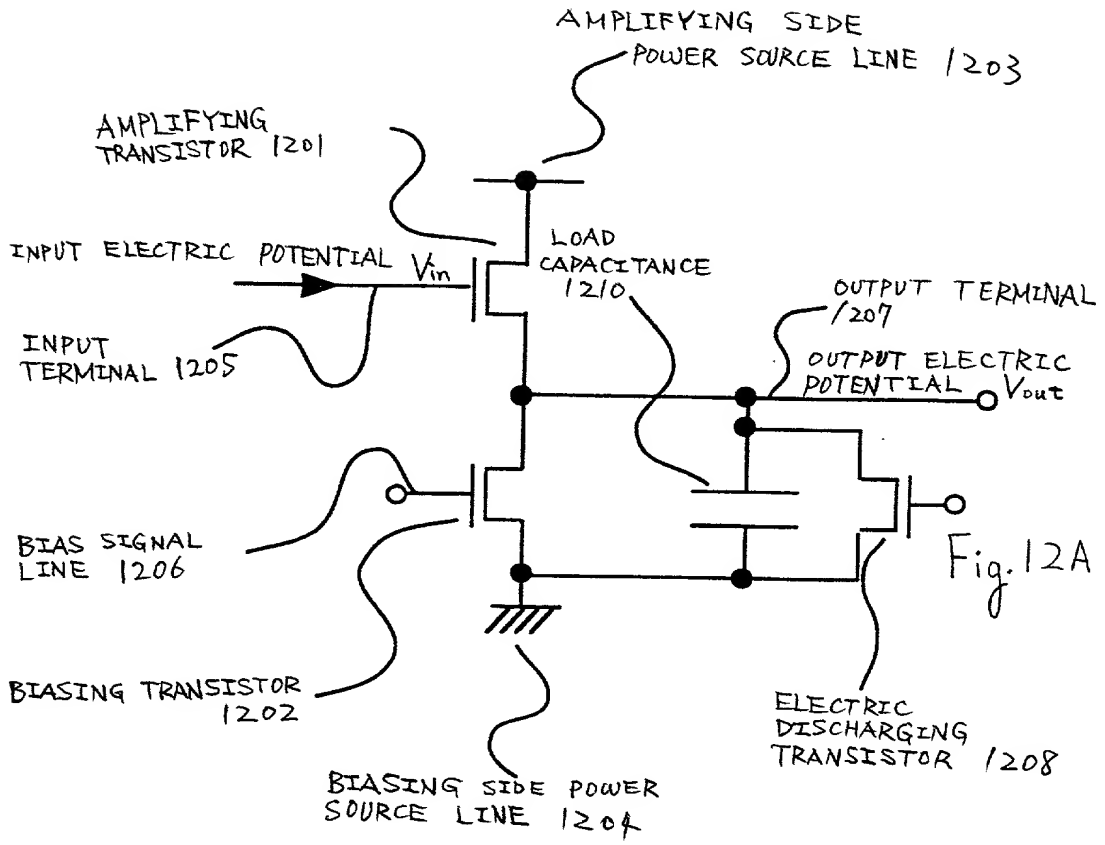


Fig. 12A

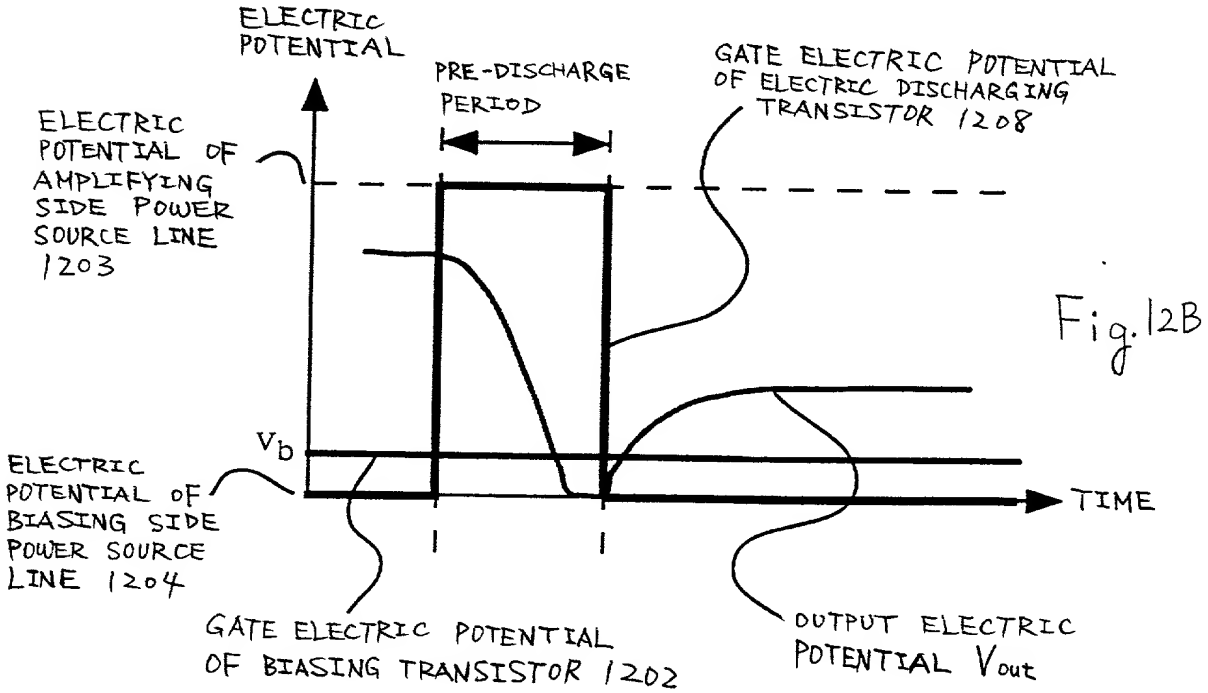


Fig. 12B

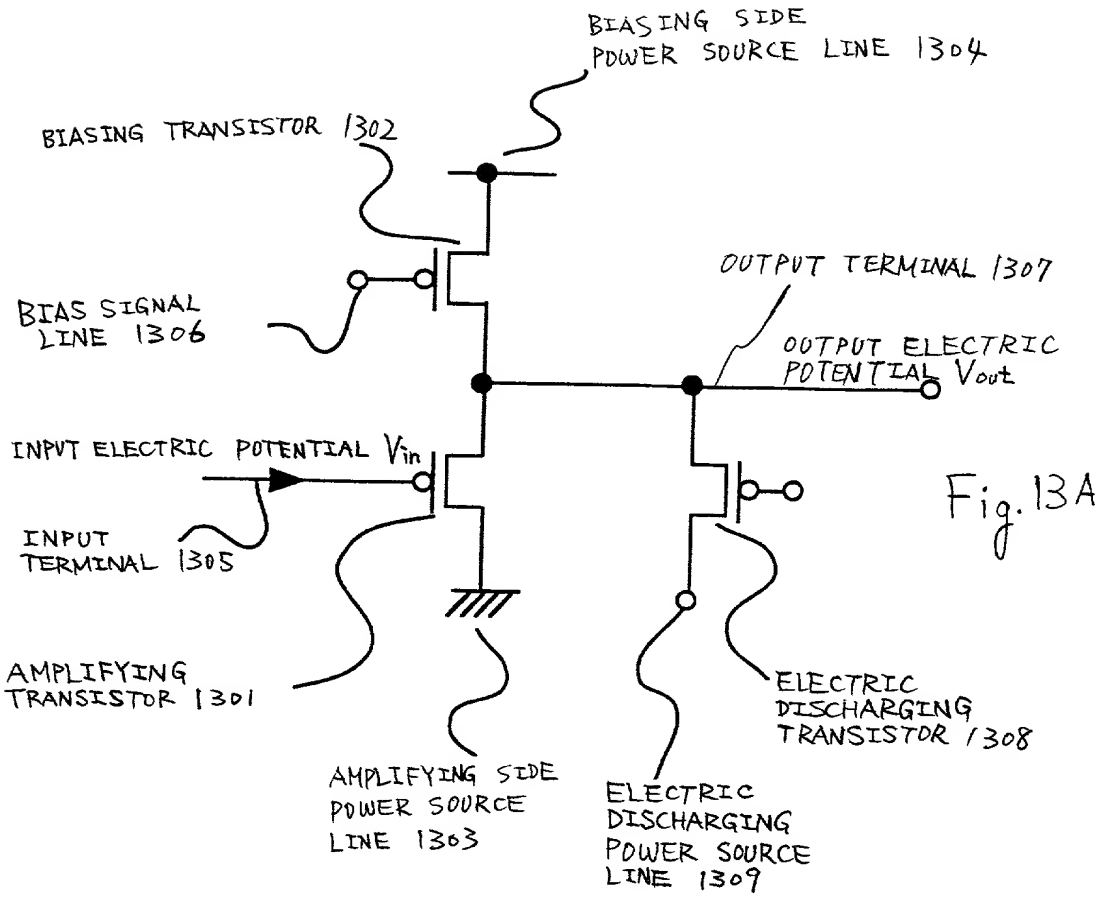


Fig. 13A

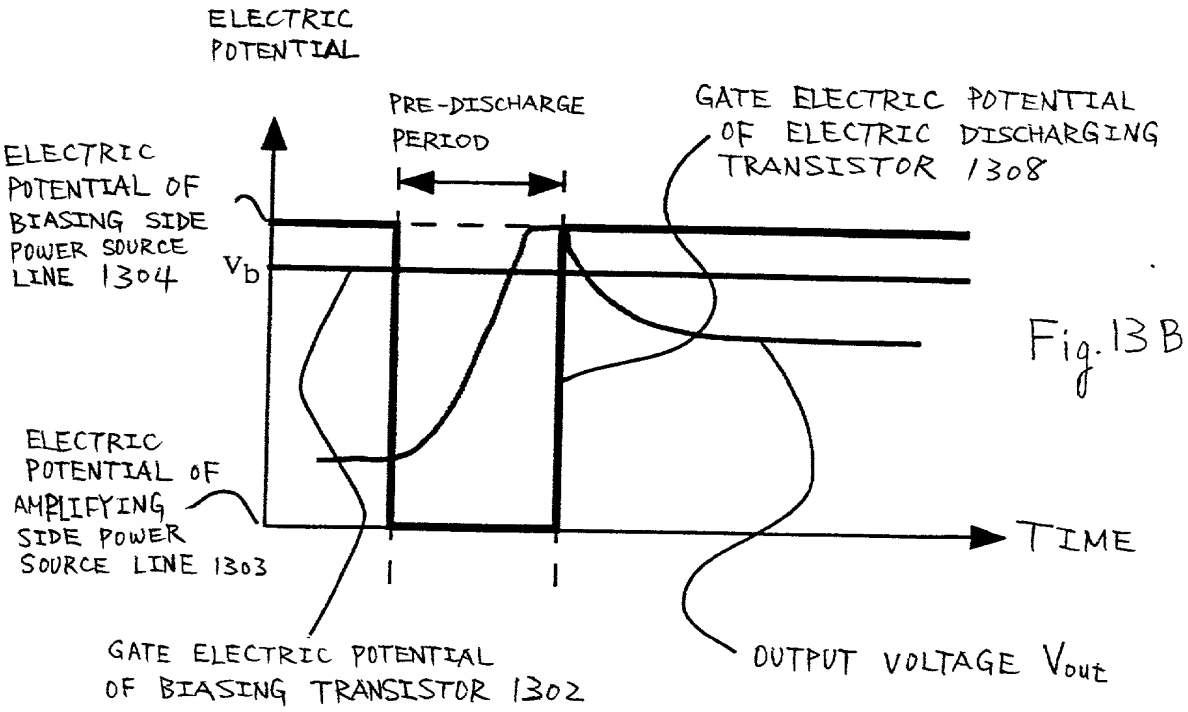


Fig. 13B

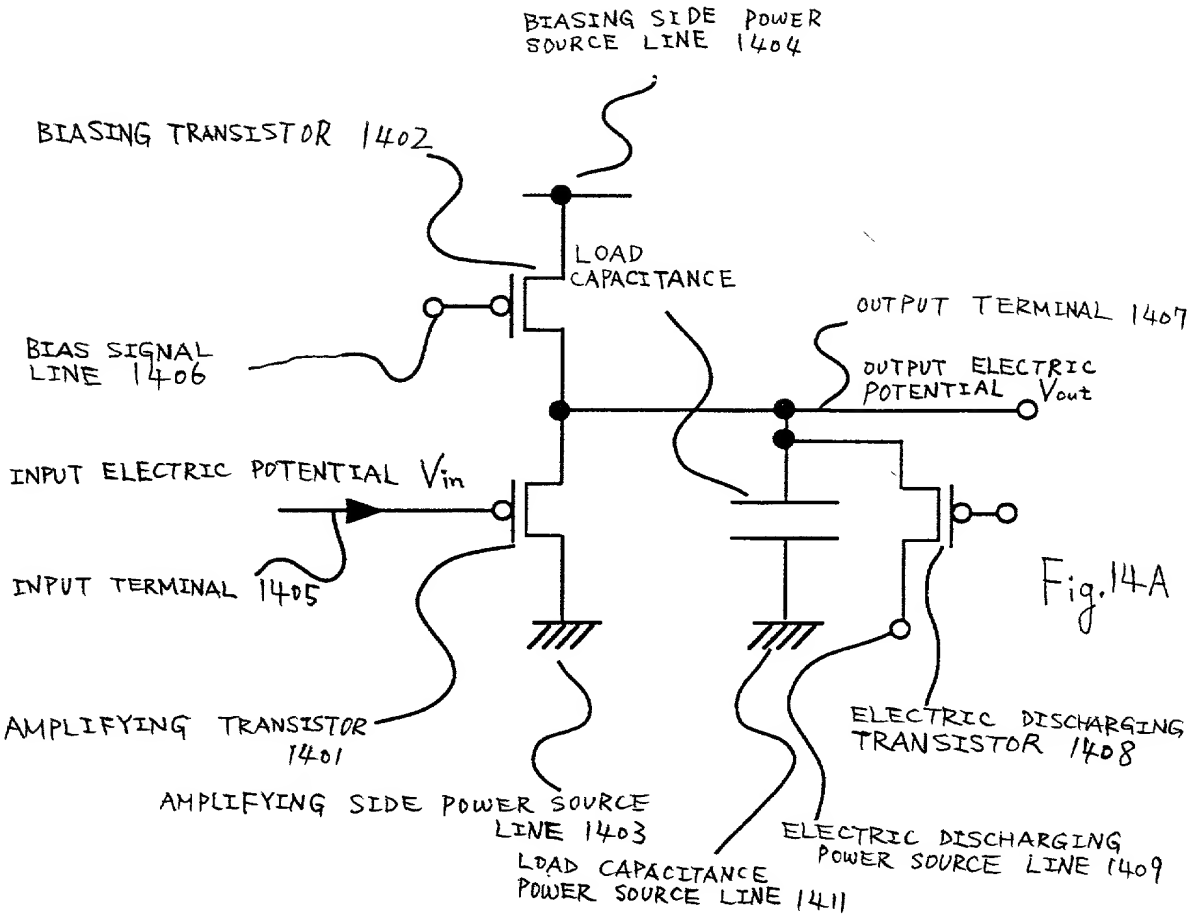


Fig. 14A

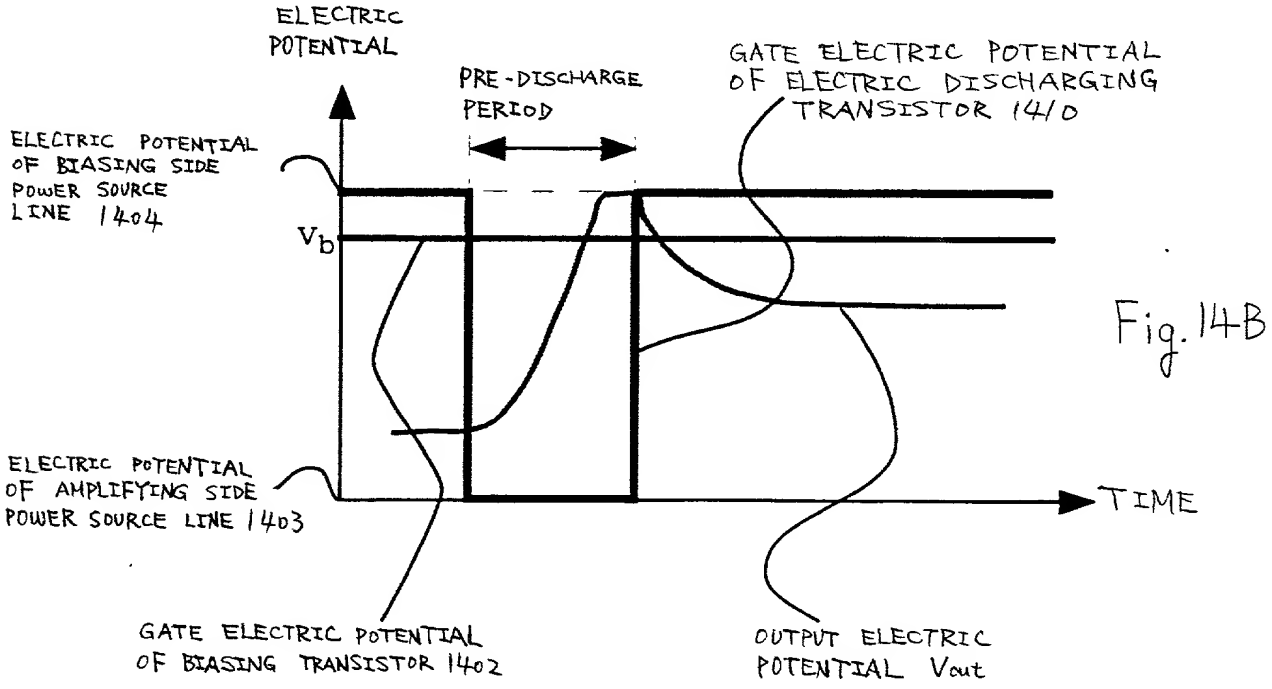


Fig. 14B

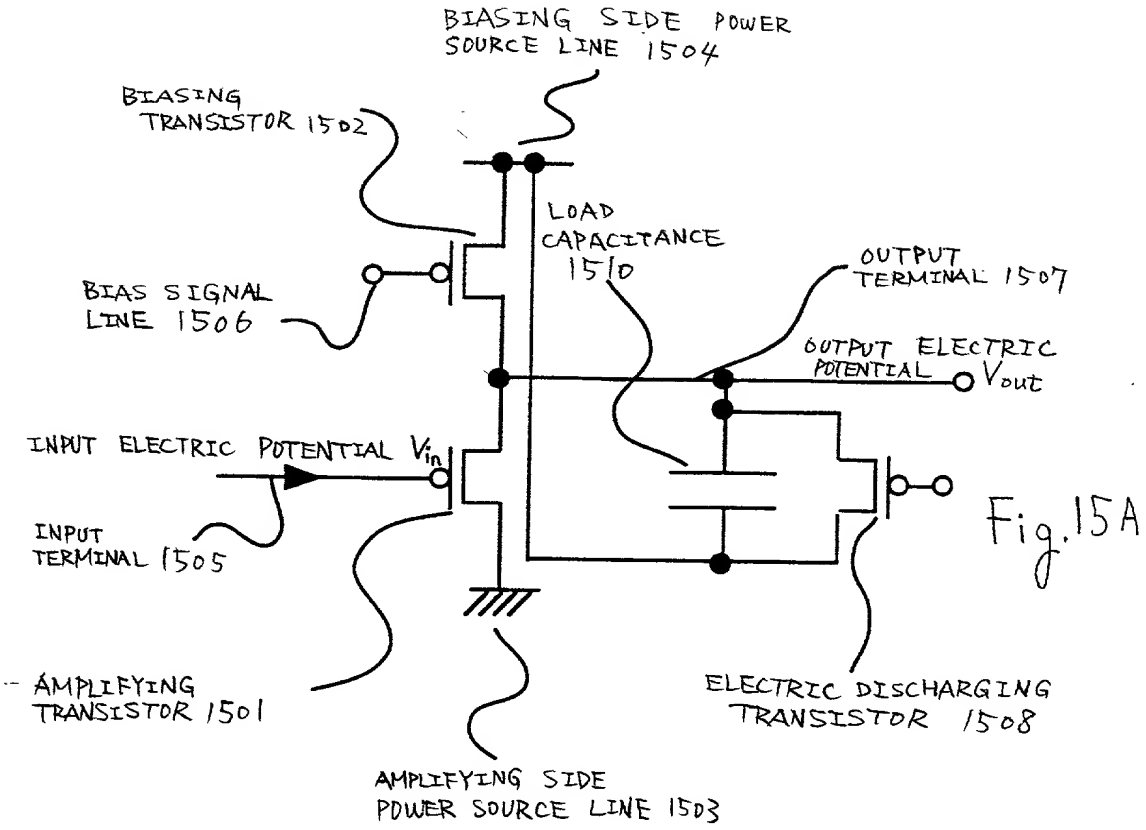


Fig. 15A

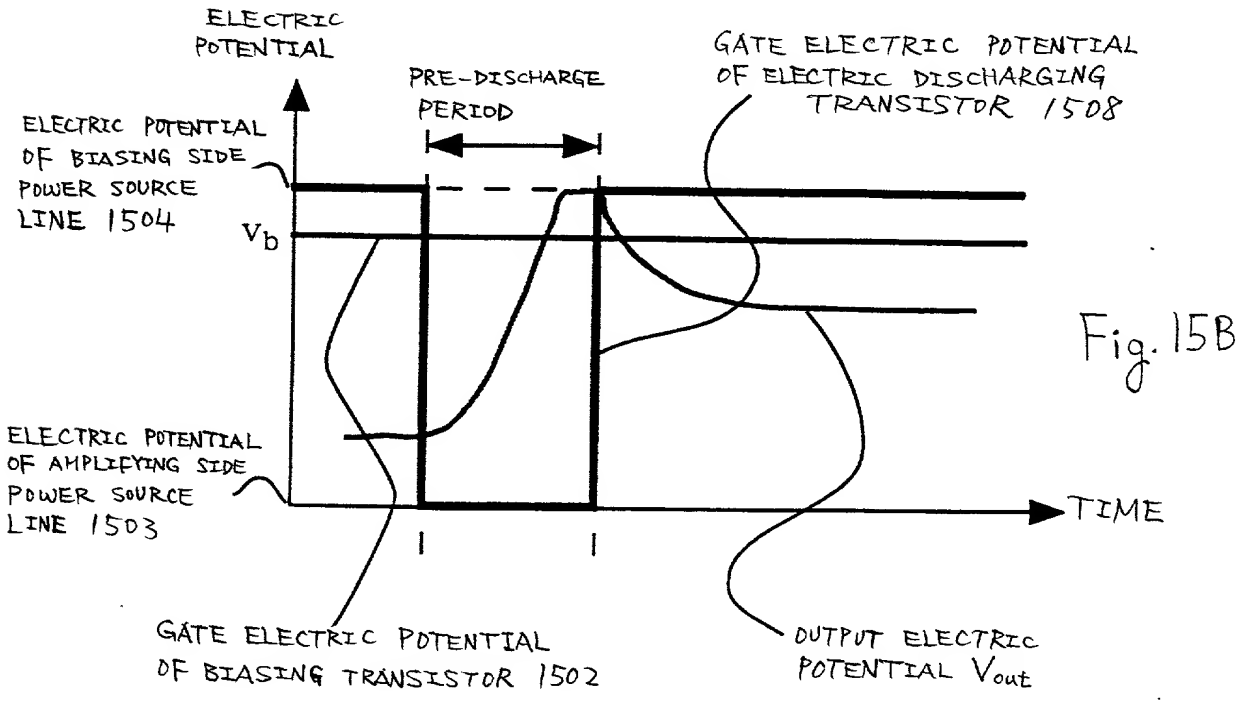


Fig. 15B

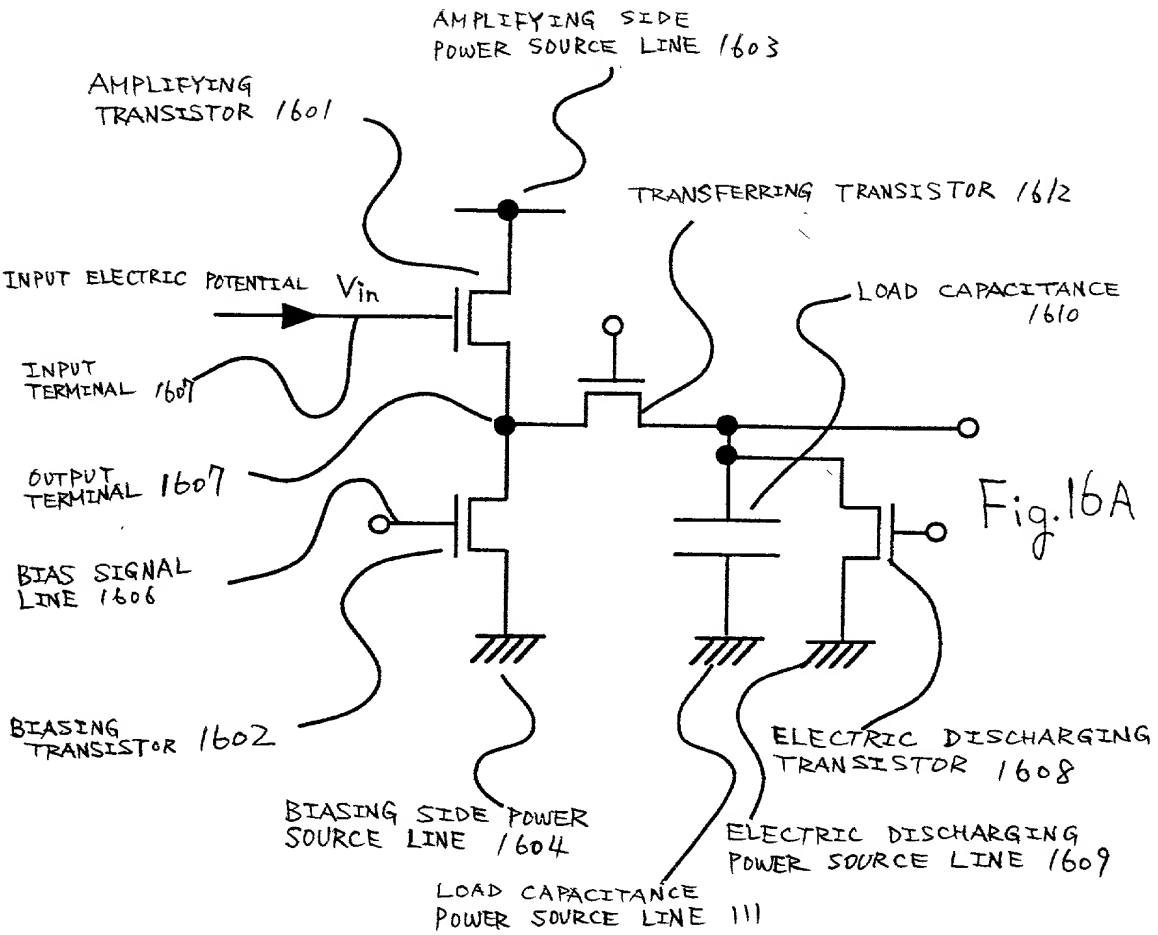


Fig.16A

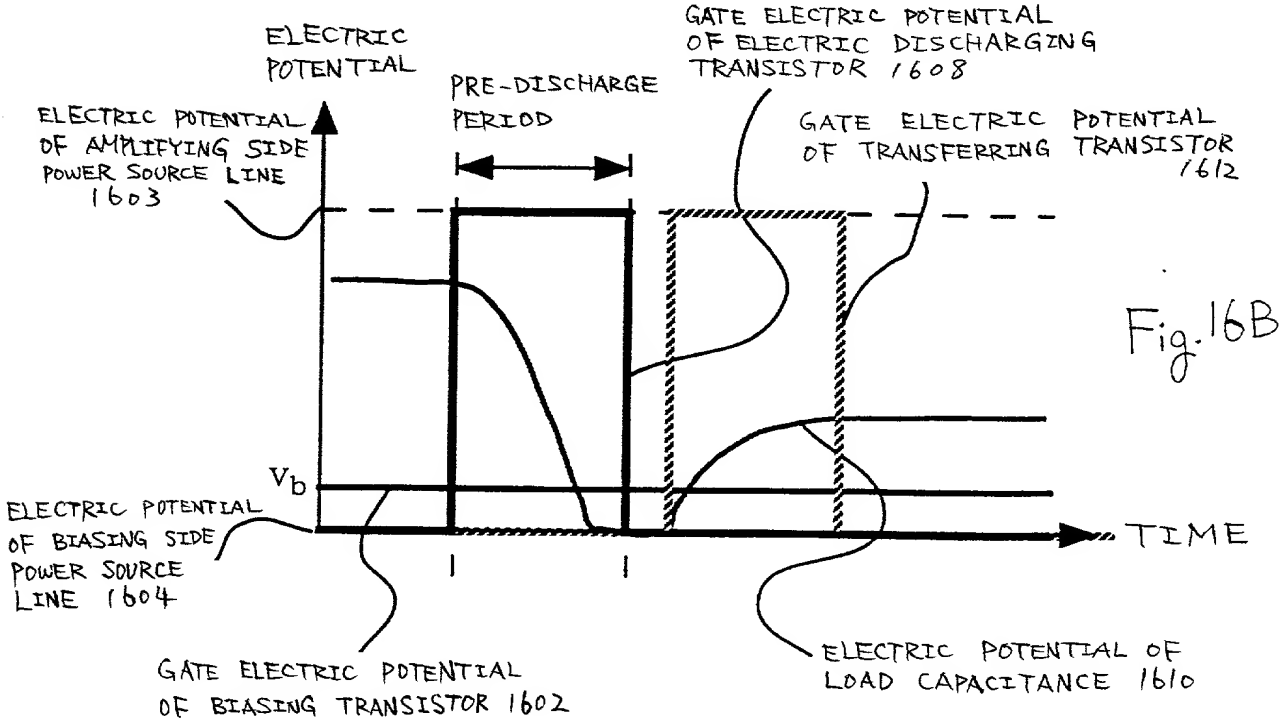


Fig.16B

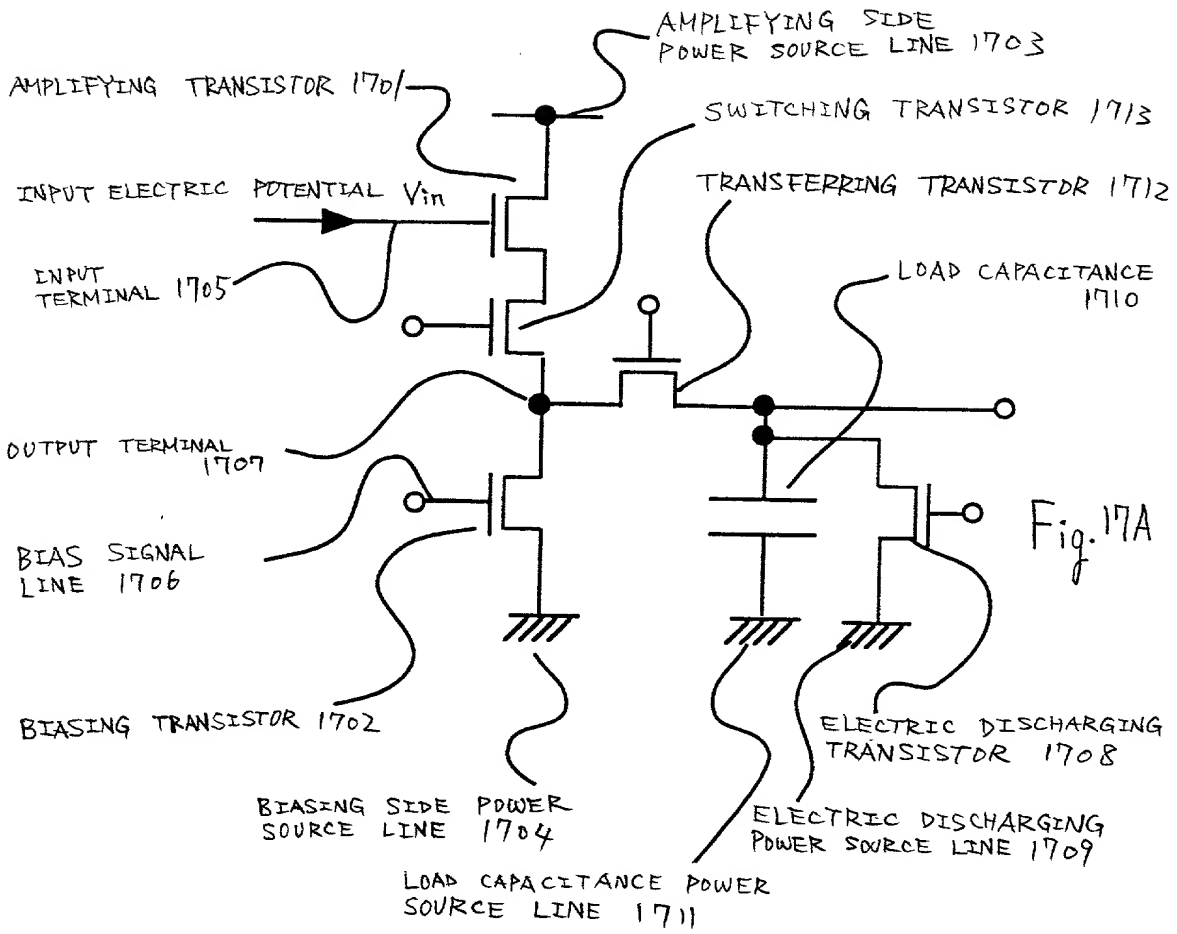


Fig. 17A

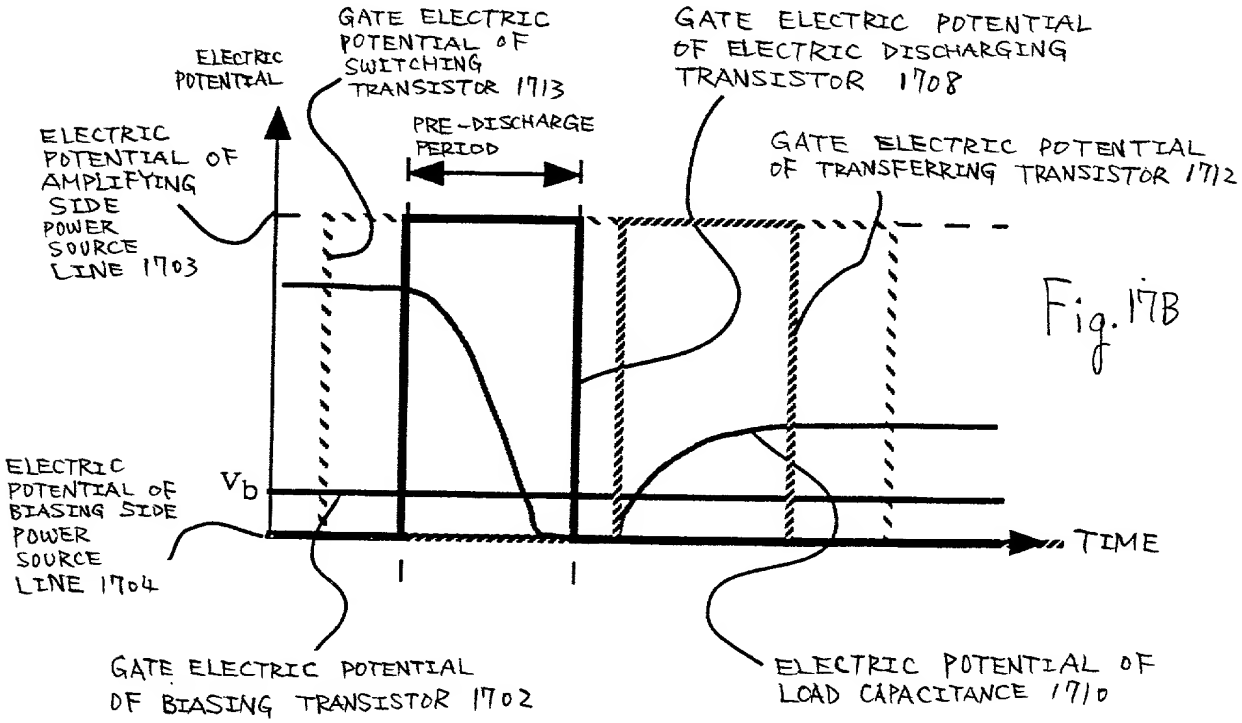


Fig. 17B

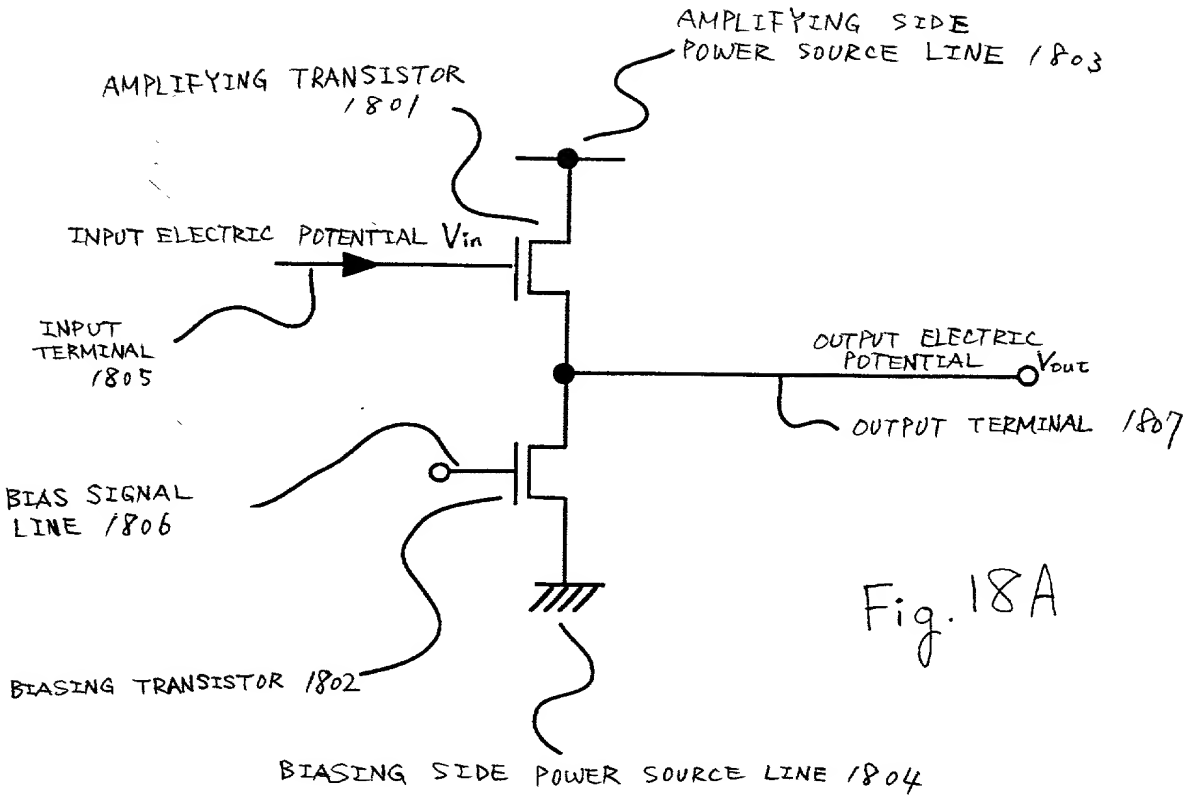


Fig. 18A

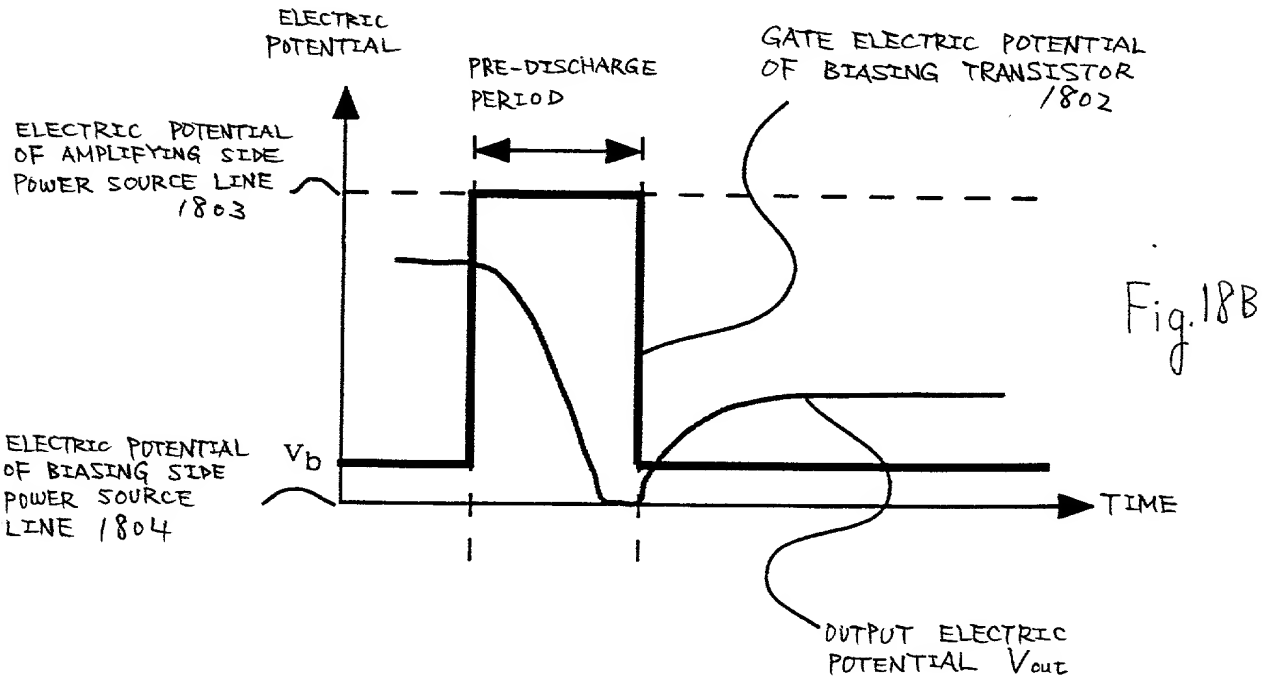


Fig. 18B

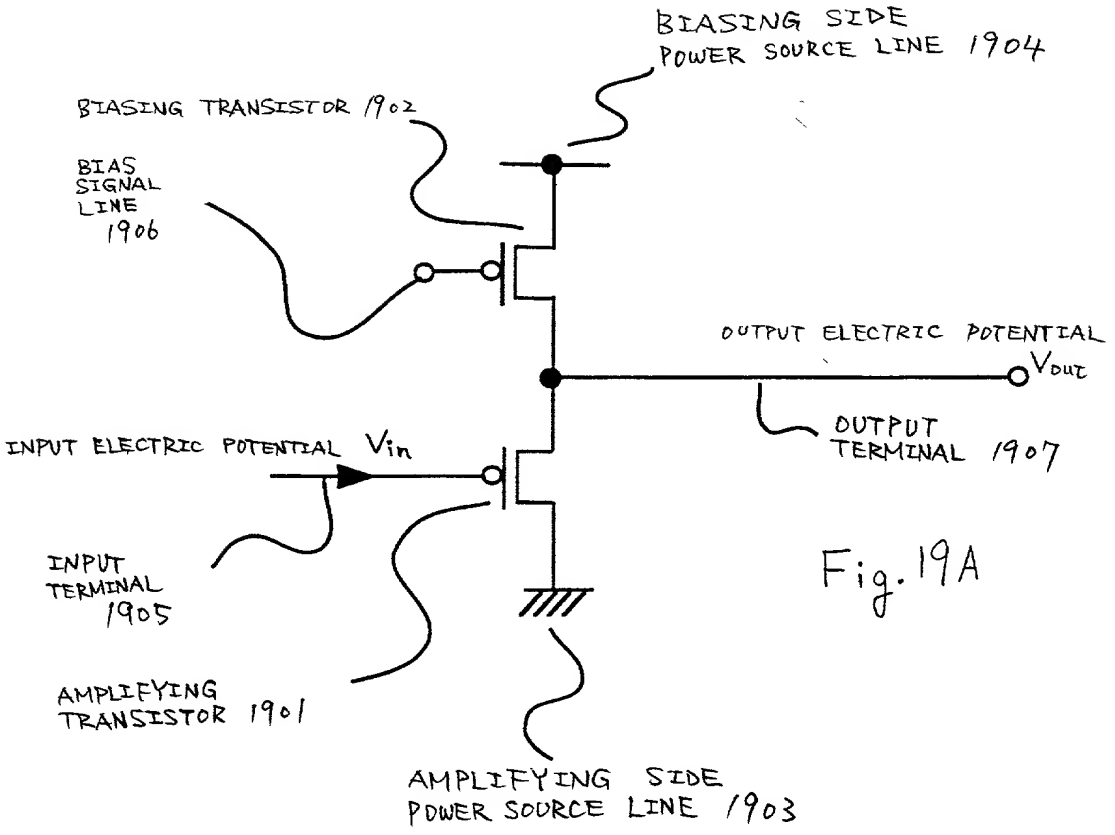


Fig. 19A

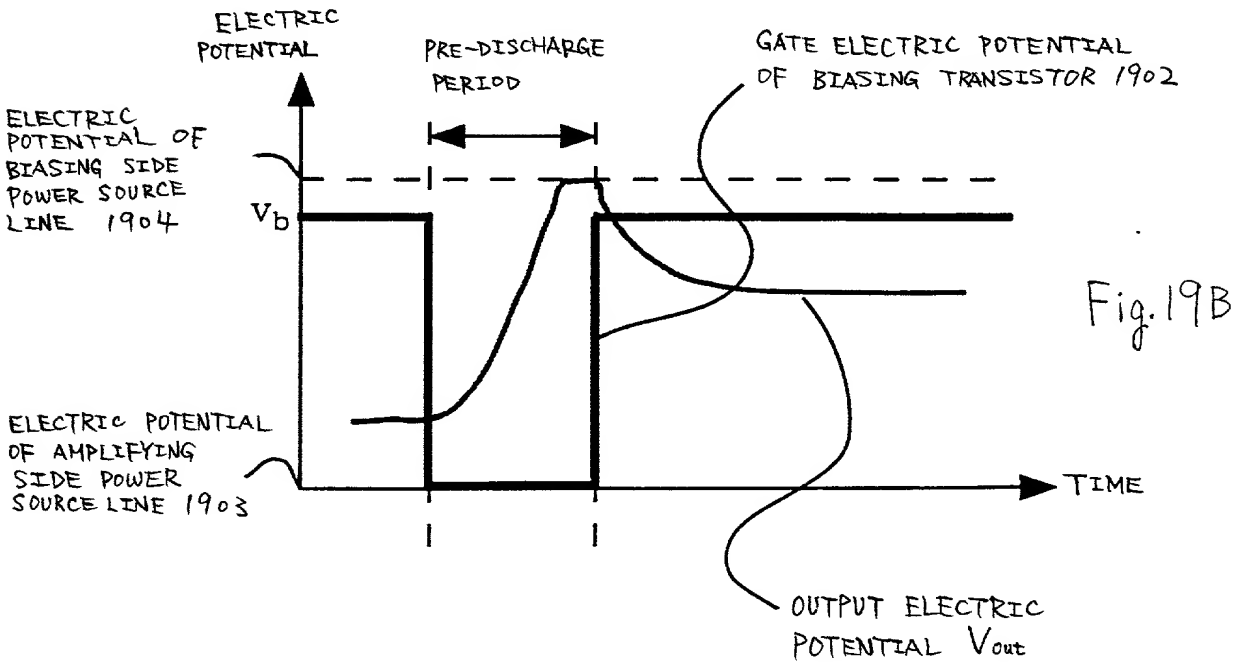


Fig. 19B

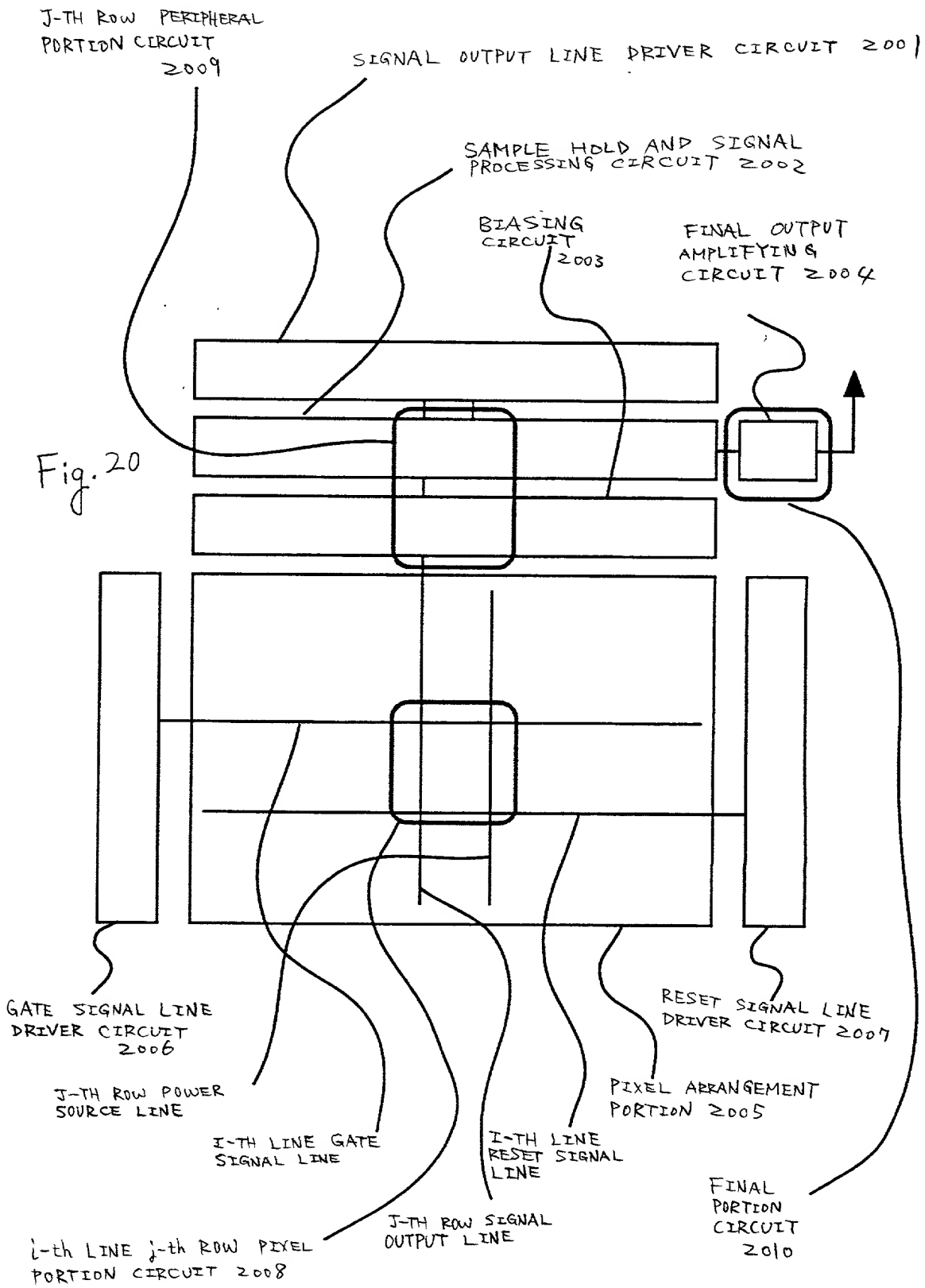

J-TH ROW PERIPHERAL PORTION CIRCUIT 2009
SIGNAL OUTPUT LINE DRIVER CIRCUIT 2001
SAMPLE HOLD AND SIGNAL PROCESSING CIRCUIT 2002
BIASING CIRCUIT 2003
FINAL OUTPUT AMPLIFYING CIRCUIT 2004
GATE SIGNAL LINE DRIVER CIRCUIT 2006
RESET SIGNAL LINE DRIVER CIRCUIT 2007
J-TH ROW POWER SOURCE LINE
I-TH LINE GATE SIGNAL LINE
I-TH LINE RESET SIGNAL LINE
PIXEL ARRANGEMENT PORTION 2005
FINAL PORTION CIRCUIT 2010
J-TH ROW SIGNAL OUTPUT LINE
i-th LINE j-th ROW PIXEL PORTION CIRCUIT 2008

Fig. 20

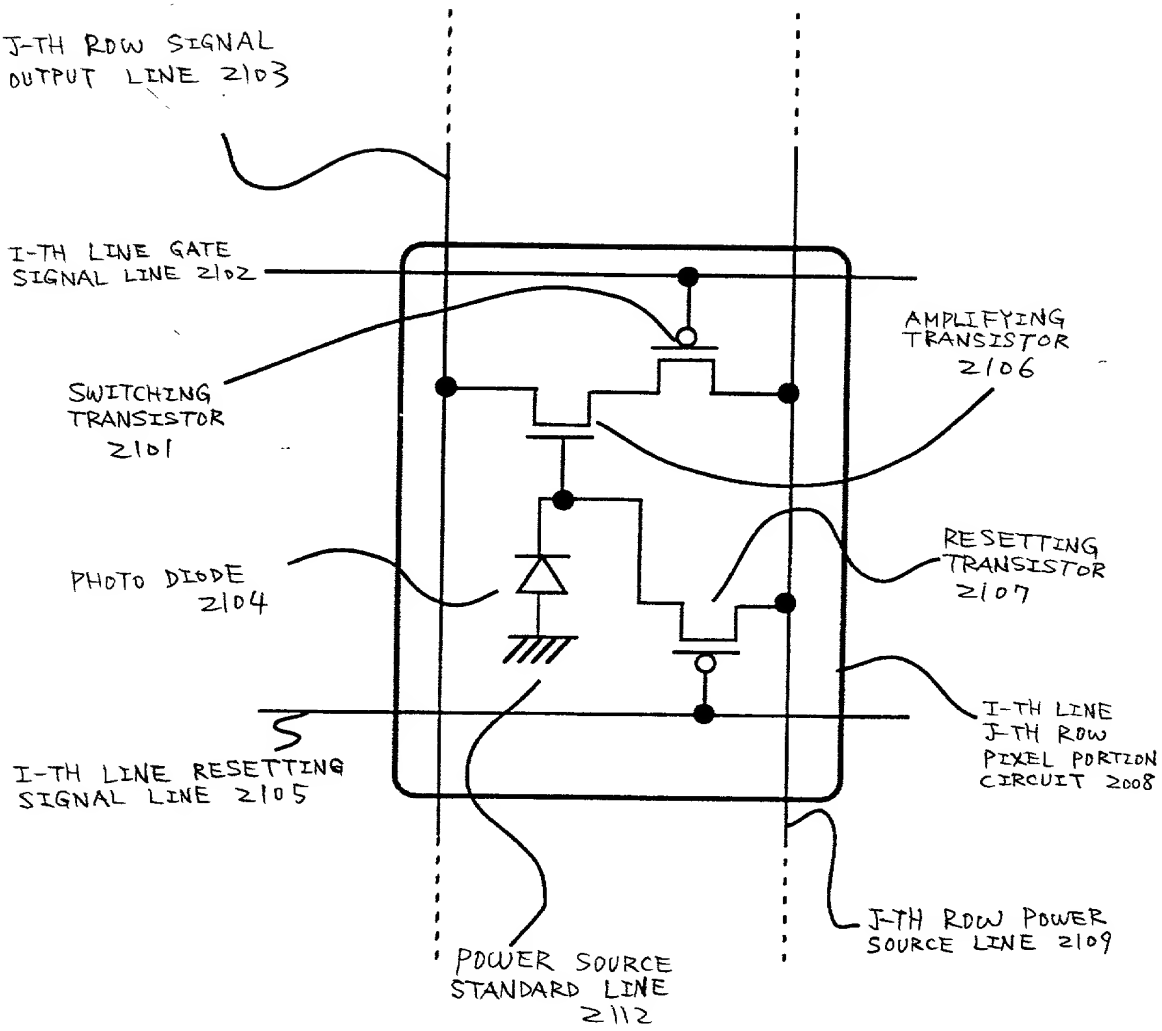

J-TH ROW SIGNAL OUTPUT LINE 2103
I-TH LINE GATE SIGNAL LINE 2102
SWITCHING TRANSISTOR 2101
AMPLIFYING TRANSISTOR 2106
PHOTO DIODE 2104
RESETTING TRANSISTOR 2107
I-TH LINE RESETTING SIGNAL LINE 2105
I-TH LINE J-TH ROW PIXEL PORTION CIRCUIT 2008
J-TH ROW POWER SOURCE LINE 2109
POWER SOURCE STANDARD LINE 2112

Fig. 21

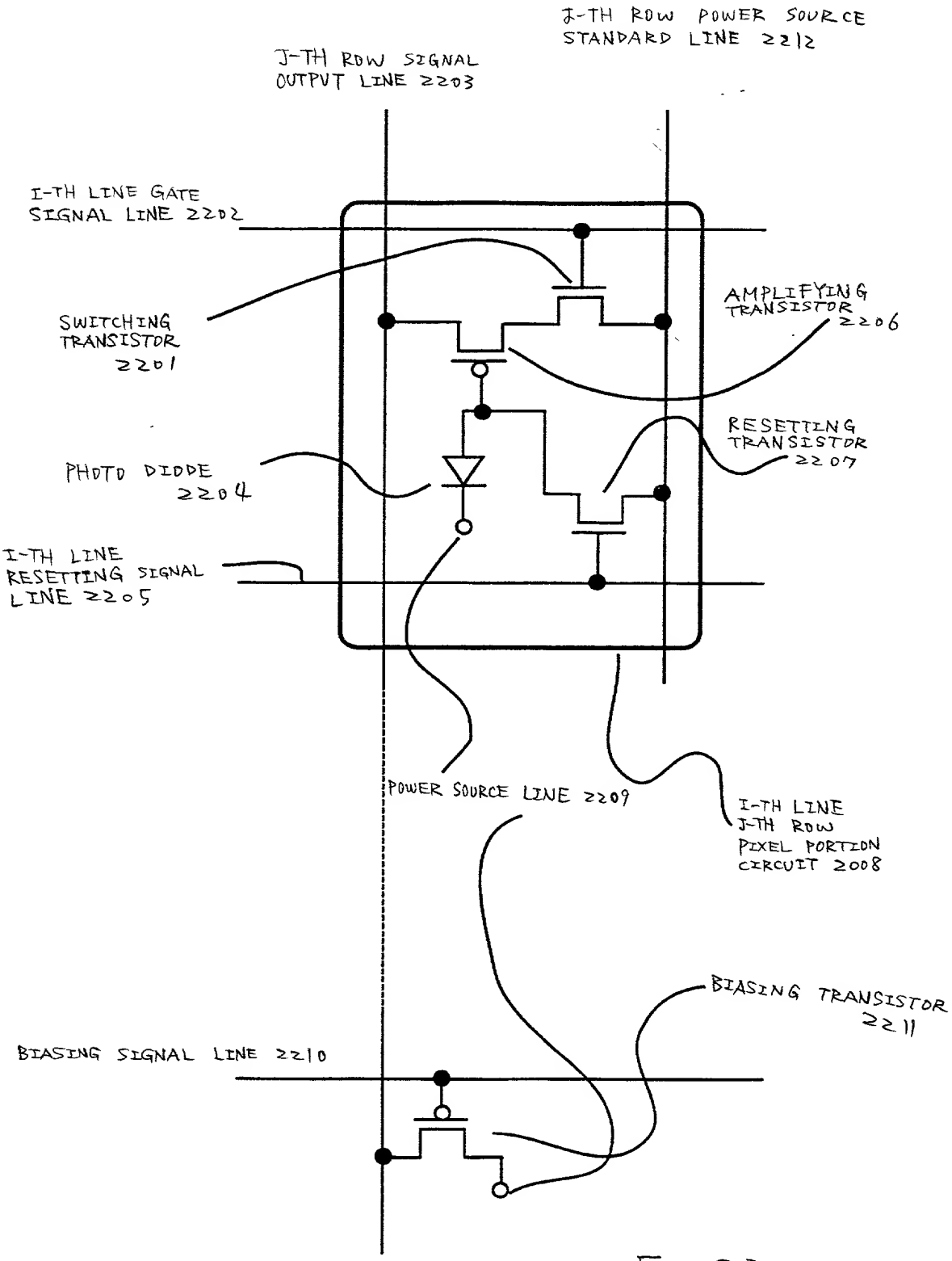

J-TH ROW POWER SOURCE STANDARD LINE 2212
J-TH ROW SIGNAL OUTPUT LINE 2203
I-TH LINE GATE SIGNAL LINE 2202
SWITCHING TRANSISTOR 2201
AMPLIFYING TRANSISTOR 2206
RESETTING TRANSISTOR 2207
PHOTO DIODE 2204
I-TH LINE RESETTING SIGNAL LINE 2205
POWER SOURCE LINE 2209
I-TH LINE J-TH ROW PIXEL PORTION CIRCUIT 2008
BIASING TRANSISTOR 2211
BIASING SIGNAL LINE 2210

Fig. 22

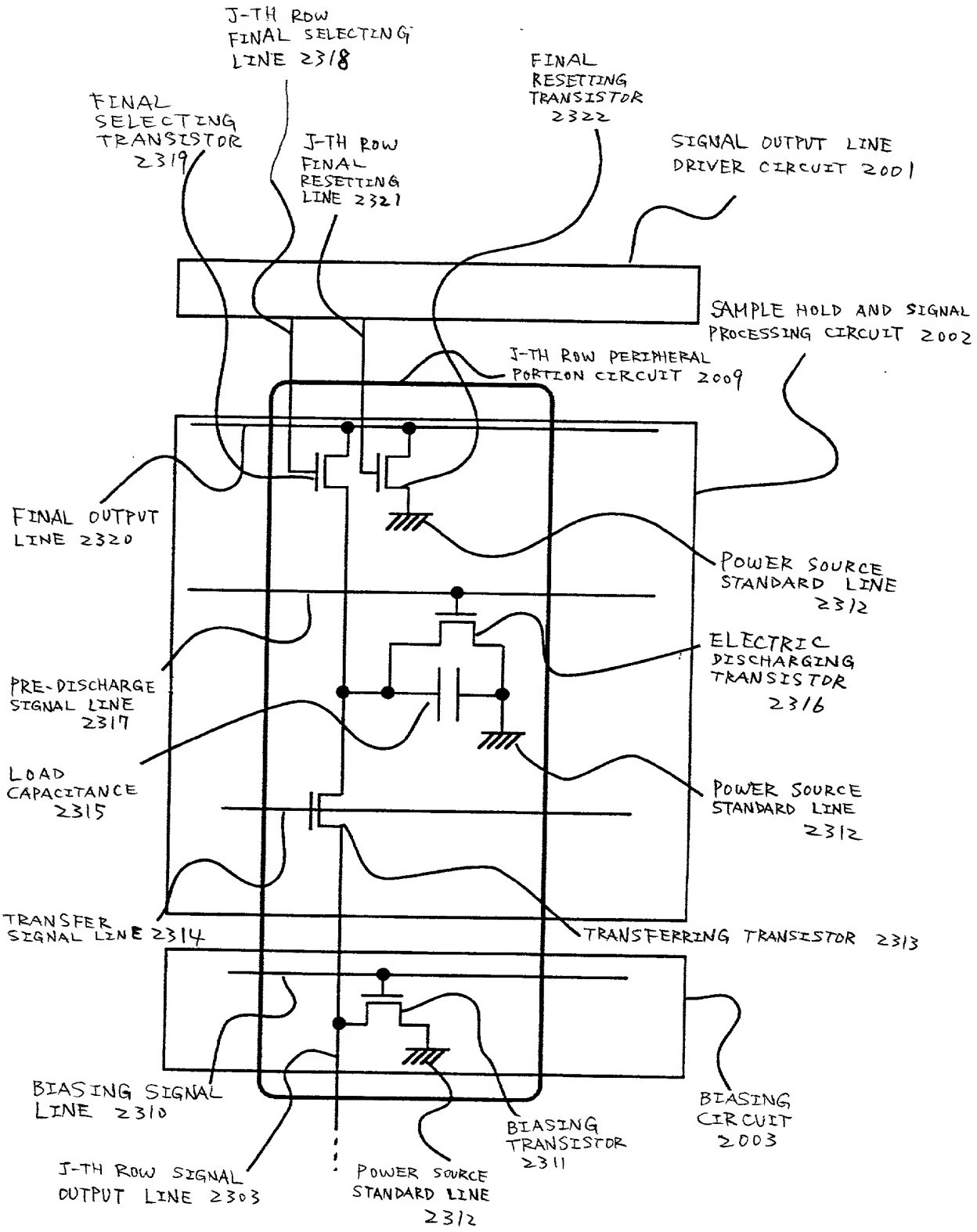

J-TH ROW FINAL SELECTING LINE 2318
FINAL SELECTING TRANSISTOR 2319
J-TH ROW FINAL RESETTING LINE 2321
FINAL RESETTING TRANSISTOR 2322
SIGNAL OUTPUT LINE DRIVER CIRCUIT 2001
SAMPLE HOLD AND SIGNAL PROCESSING CIRCUIT 2002
J-TH ROW PERIPHERAL PORTION CIRCUIT 2009
FINAL OUTPUT LINE 2320
POWER SOURCE STANDARD LINE 2312
ELECTRIC DISCHARGING TRANSISTOR 2316
PRE-DISCHARGE SIGNAL LINE 2317
LOAD CAPACITANCE 2315
POWER SOURCE STANDARD LINE 2312
TRANSFER SIGNAL LINE 2314
TRANSFERRING TRANSISTOR 2313
BIASING SIGNAL LINE 2310
BIASING CIRCUIT 2003
BIASING TRANSISTOR 2311
J-TH ROW SIGNAL OUTPUT LINE 2303
POWER SOURCE STANDARD LINE 2312

Fig. 23

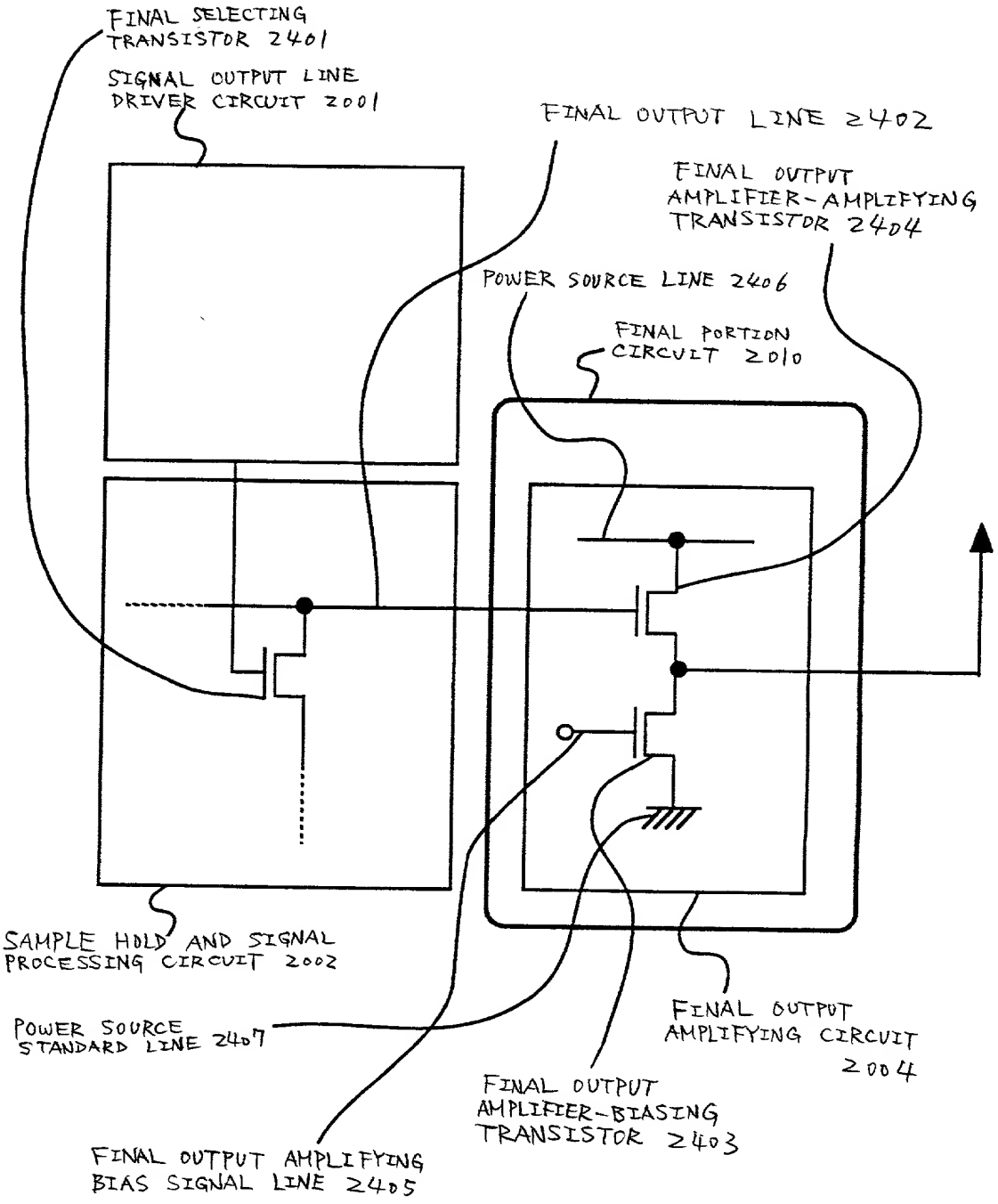

FINAL SELECTING TRANSISTOR 2401
SIGNAL OUTPUT LINE DRIVER CIRCUIT 2001
FINAL OUTPUT LINE 2402
FINAL OUTPUT AMPLIFIER-AMPLIFYING TRANSISTOR 2404
POWER SOURCE LINE 2406
FINAL PORTION CIRCUIT 2010
SAMPLE HOLD AND SIGNAL PROCESSING CIRCUIT 2002
POWER SOURCE STANDARD LINE 2407
FINAL OUTPUT AMPLIFYING CIRCUIT 2004
FINAL OUTPUT AMPLIFIER-BIASING TRANSISTOR 2403
FINAL OUTPUT AMPLIFYING BIAS SIGNAL LINE 2405

Fig. 24

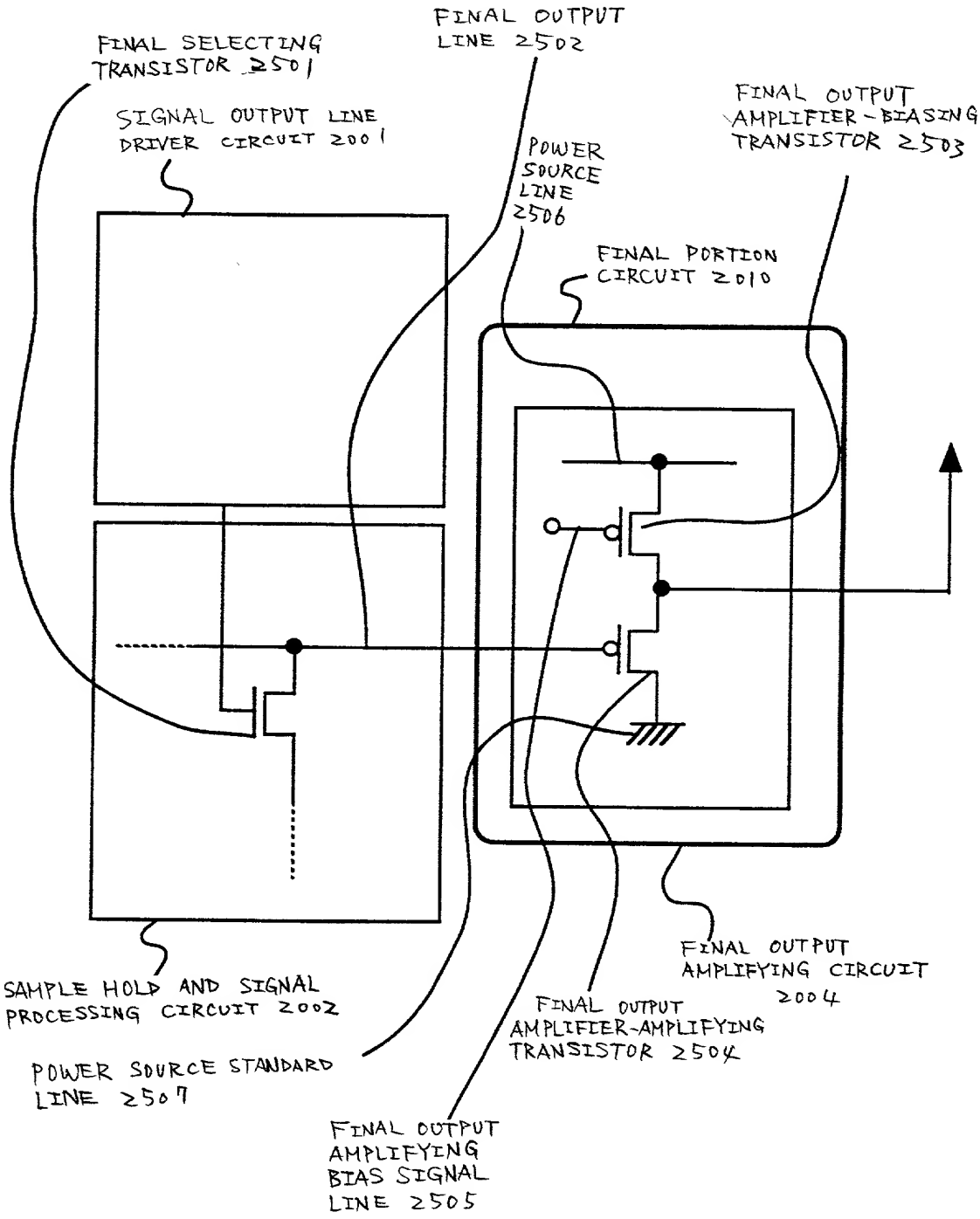

FINAL SELECTING TRANSISTOR 2501
FINAL OUTPUT LINE 2502
SIGNAL OUTPUT LINE DRIVER CIRCUIT 2001
POWER SOURCE LINE 2506
FINAL OUTPUT AMPLIFIER-BIASING TRANSISTOR 2503
FINAL PORTION CIRCUIT 2010
SAMPLE HOLD AND SIGNAL PROCESSING CIRCUIT 2002
POWER SOURCE STANDARD LINE 2507
FINAL OUTPUT AMPLIFYING BIAS SIGNAL LINE 2505
FINAL OUTPUT AMPLIFIER-AMPLIFYING TRANSISTOR 2504
FINAL OUTPUT AMPLIFYING CIRCUIT 2004

Fig. 25

Fig. 26

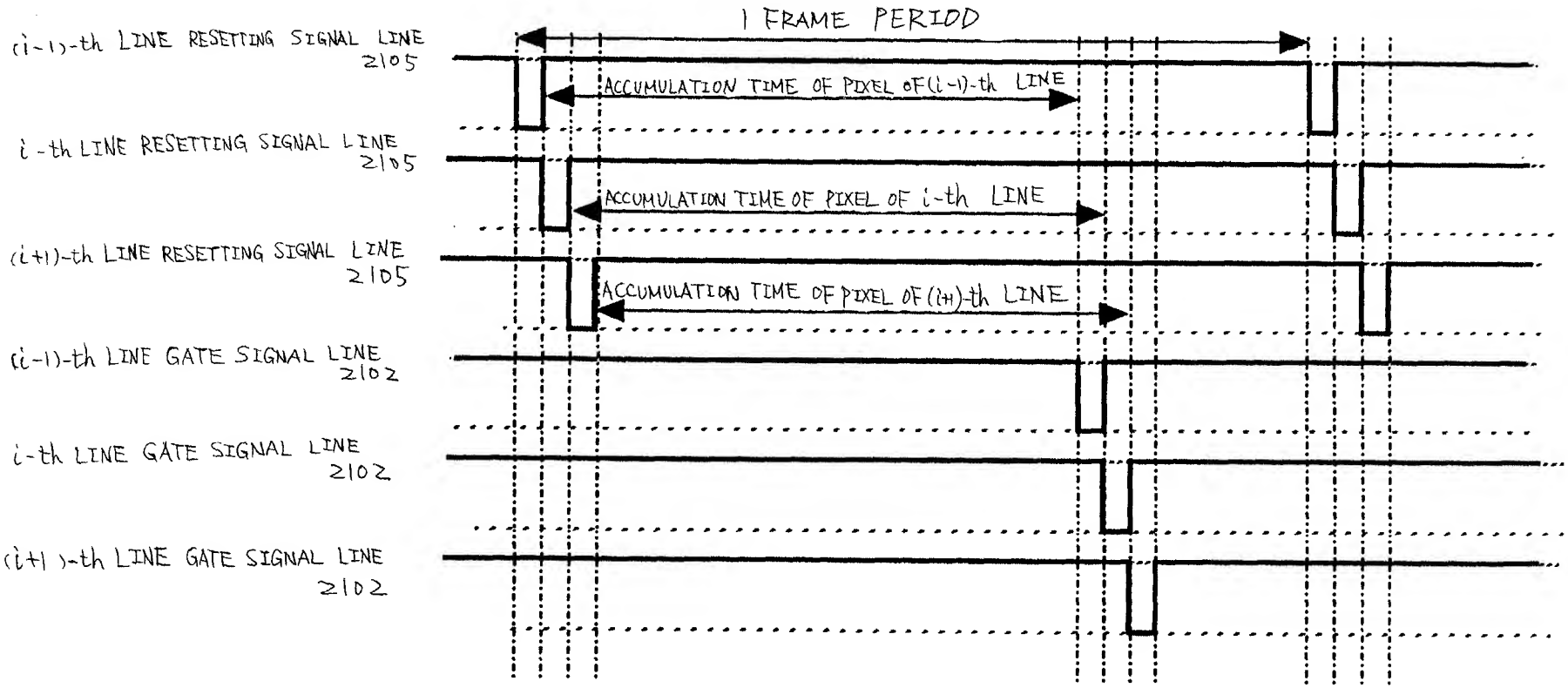
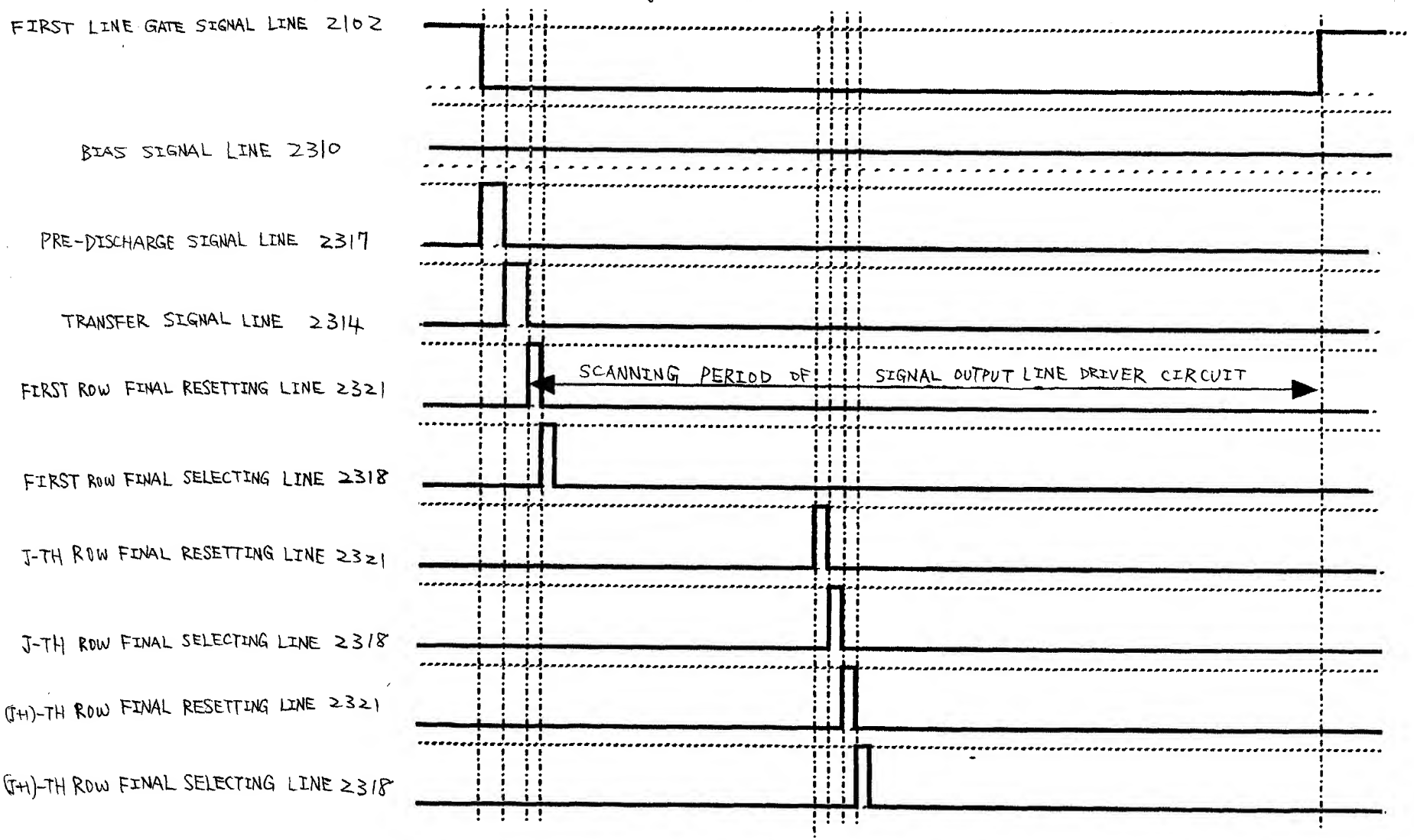
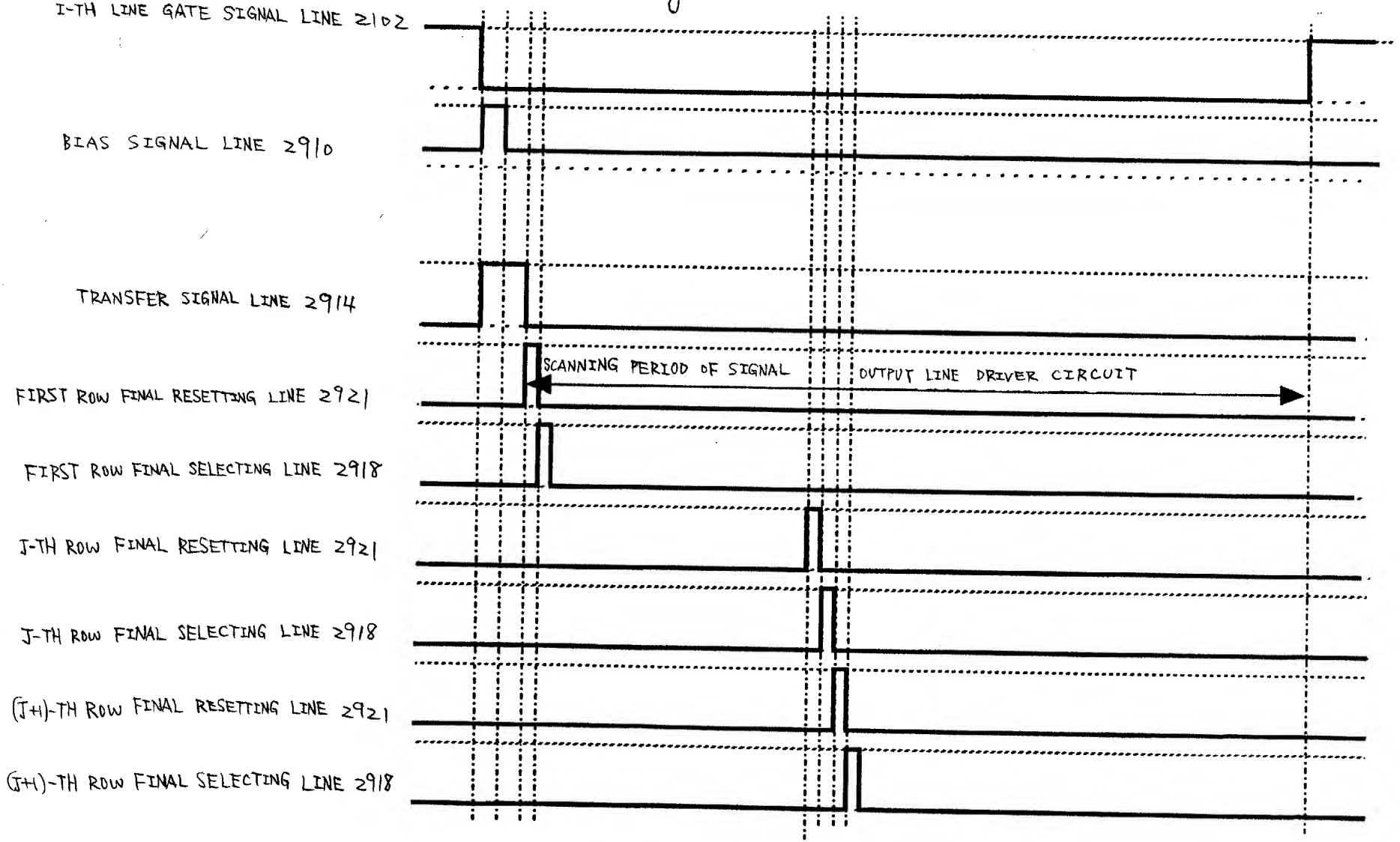

1 FRAME PERIOD
(i-1)-th LINE RESETTING SIGNAL LINE 2105
ACCUMULATION TIME OF PIXEL OF (i-1)-th LINE
i-th LINE RESETTING SIGNAL LINE 2105
ACCUMULATION TIME OF PIXEL OF i-th LINE
(i+1)-th LINE RESETTING SIGNAL LINE 2105
ACCUMULATION TIME OF PIXEL OF (i+1)-th LINE
(i-1)-th LINE GATE SIGNAL LINE 2102
i-th LINE GATE SIGNAL LINE 2102
(i+1)-th LINE GATE SIGNAL LINE 2102

Fig. 27


FIRST LINE GATE SIGNAL LINE 2102
BIAS SIGNAL LINE 2310
PRE-DISCHARGE SIGNAL LINE 2317
TRANSFER SIGNAL LINE 2314
FIRST ROW FINAL RESETTING LINE 2321
SCANNING PERIOD OF SIGNAL OUTPUT LINE DRIVER CIRCUIT
FIRST ROW FINAL SELECTING LINE 2318
J-TH ROW FINAL RESETTING LINE 2321
J-TH ROW FINAL SELECTING LINE 2318
(J+1)-TH ROW FINAL RESETTING LINE 2321
(J+1)-TH ROW FINAL SELECTING LINE 2318

DISCLOSED UNDER 35 U.S.C. 122(b)

Fig. 28



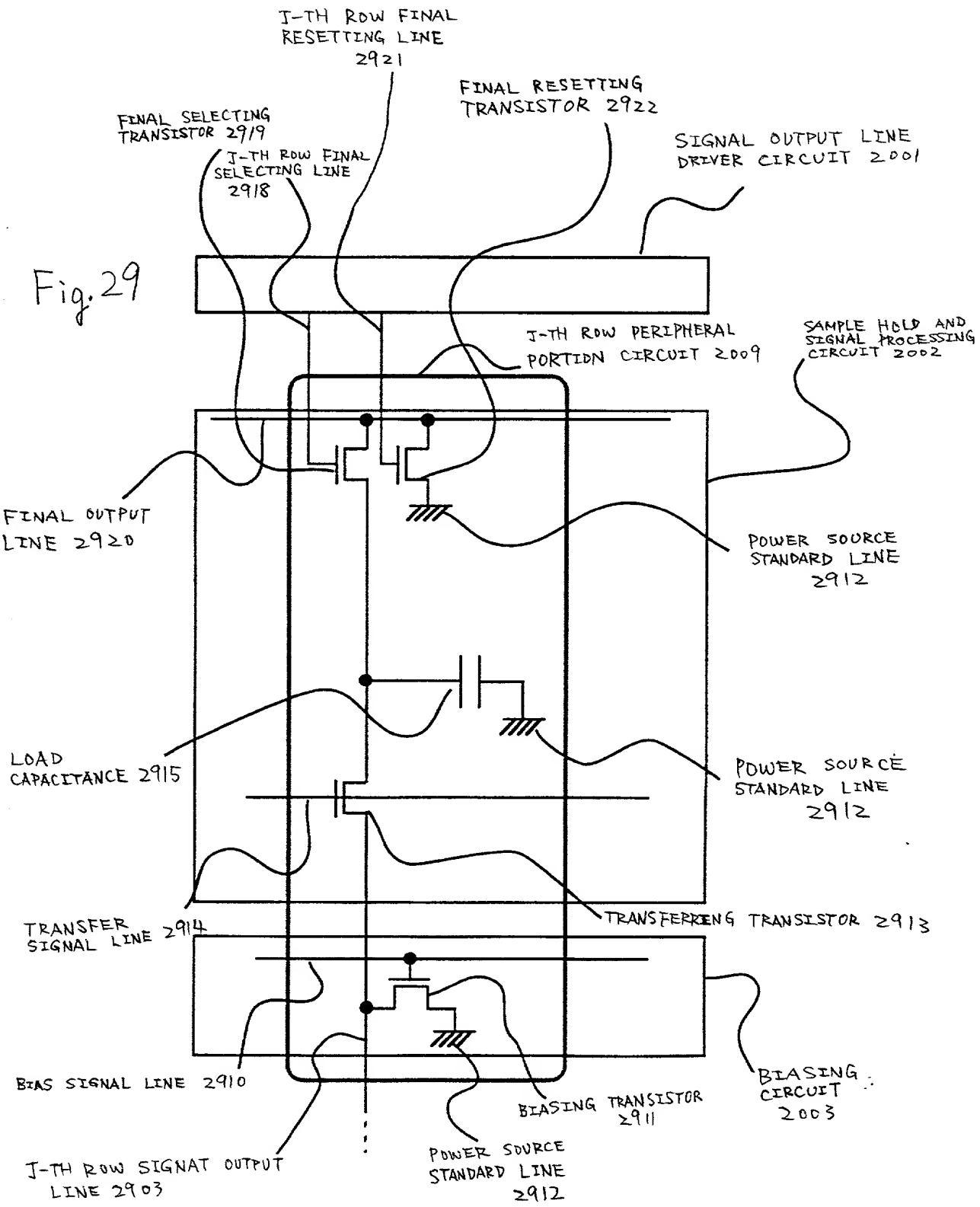

J-TH ROW FINAL RESETTING LINE 2921
FINAL RESETTING TRANSISTOR 2922
FINAL SELECTING TRANSISTOR 2919
J-TH ROW FINAL SELECTING LINE 2918
SIGNAL OUTPUT LINE DRIVER CIRCUIT 2001
J-TH ROW PERIPHERAL PORTION CIRCUIT 2009
SAMPLE HOLD AND SIGNAL PROCESSING CIRCUIT 2002
FINAL OUTPUT LINE 2920
POWER SOURCE STANDARD LINE 2912
LOAD CAPACITANCE 2915
POWER SOURCE STANDARD LINE 2912
TRANSFER SIGNAL LINE 2914
TRANSFERRING TRANSISTOR 2913
BIAS SIGNAL LINE 2910
BIASING TRANSISTOR 2911
BIASING CIRCUIT 2003
J-TH ROW SIGNAT OUTPUT LINE 2903
POWER SOURCE STANDARD LINE 2912

Fig. 29

Fig. 30A CRYSTALLIZATION STEP

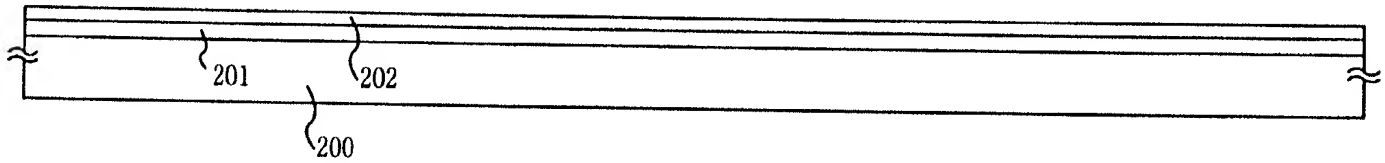


Fig. 30B

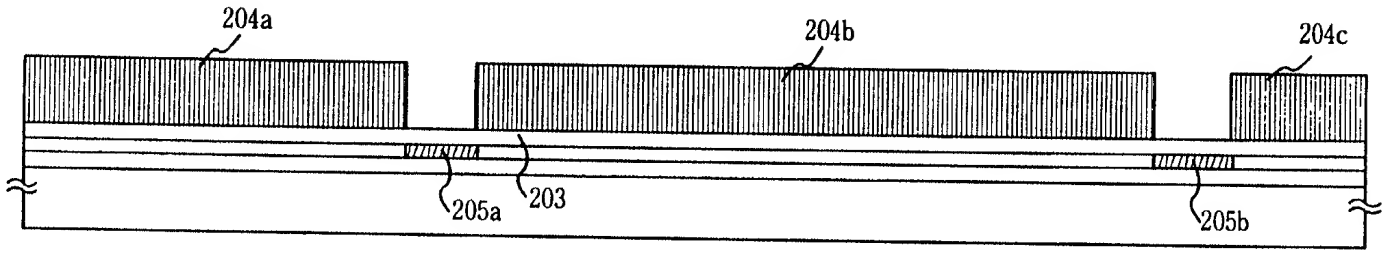


Fig. 30C LASER ANNEALING STEP

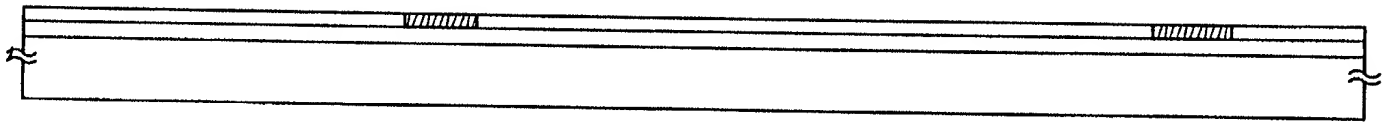


Fig. 30D

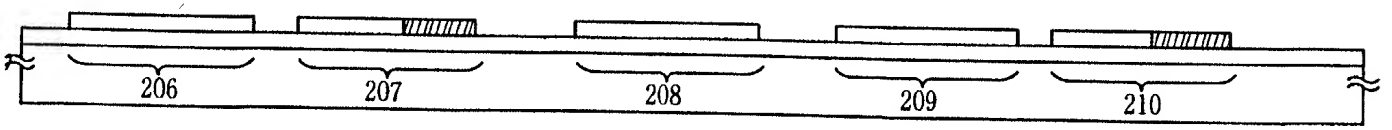


Fig. 31A

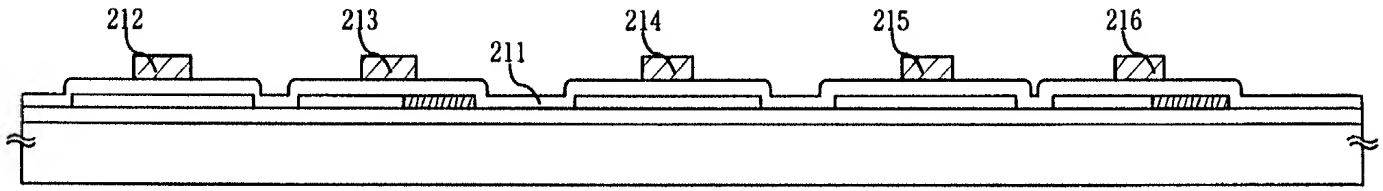


Fig. 31B

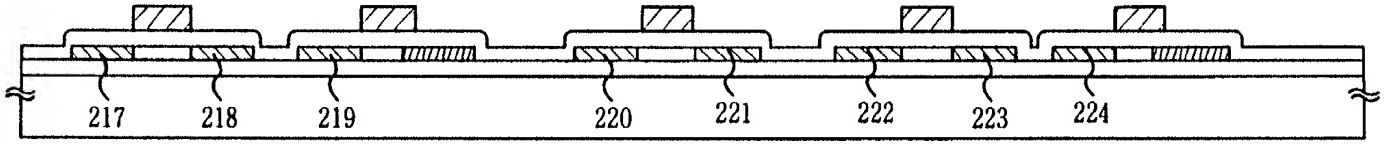


Fig. 31C

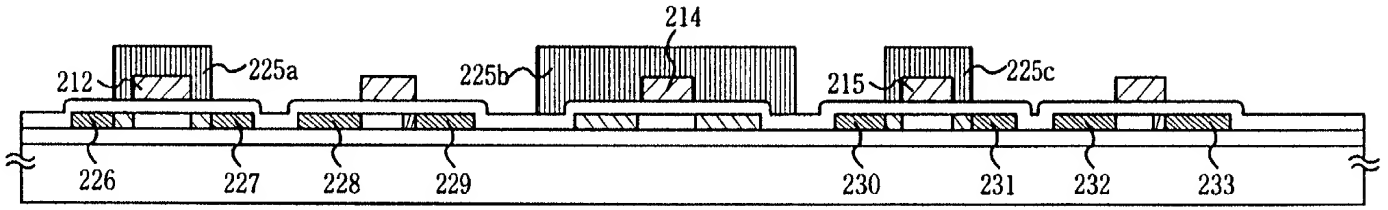


Fig. 31D

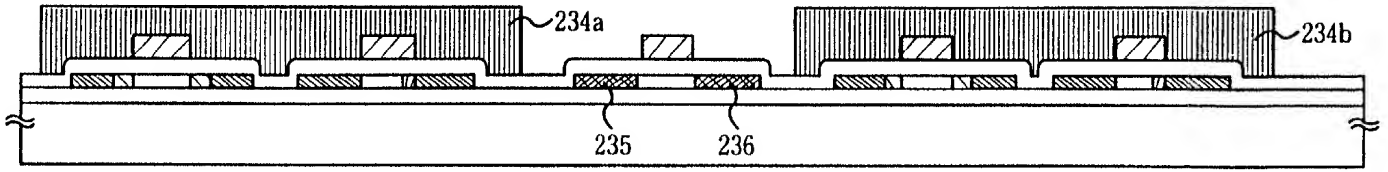


Fig.32A

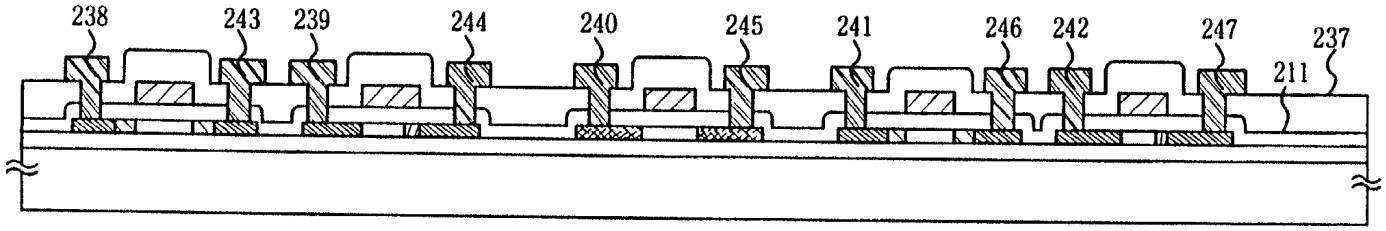


Fig.32B

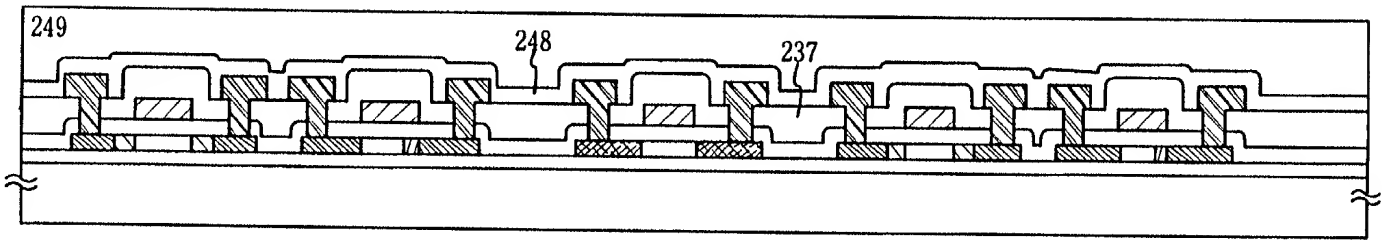


Fig.32C

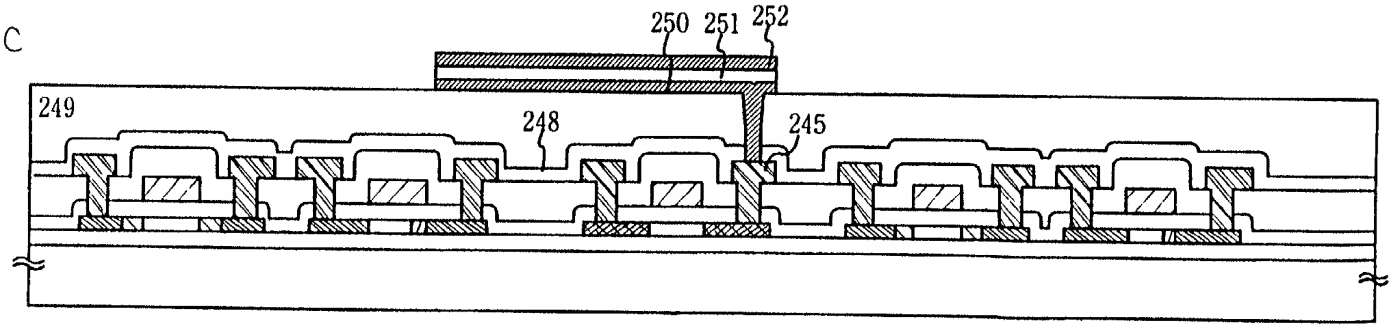


Fig. 33A

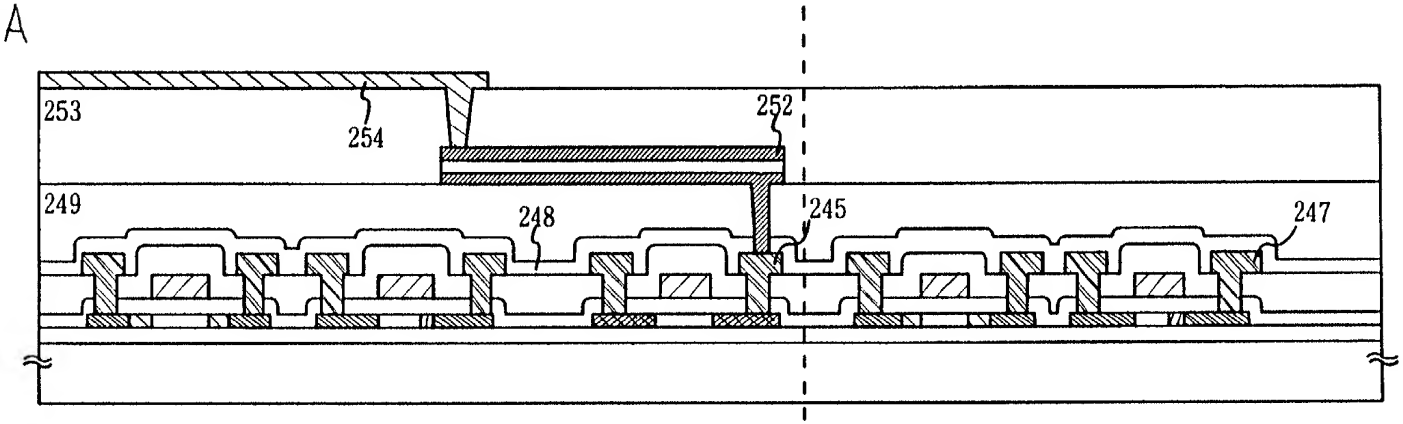
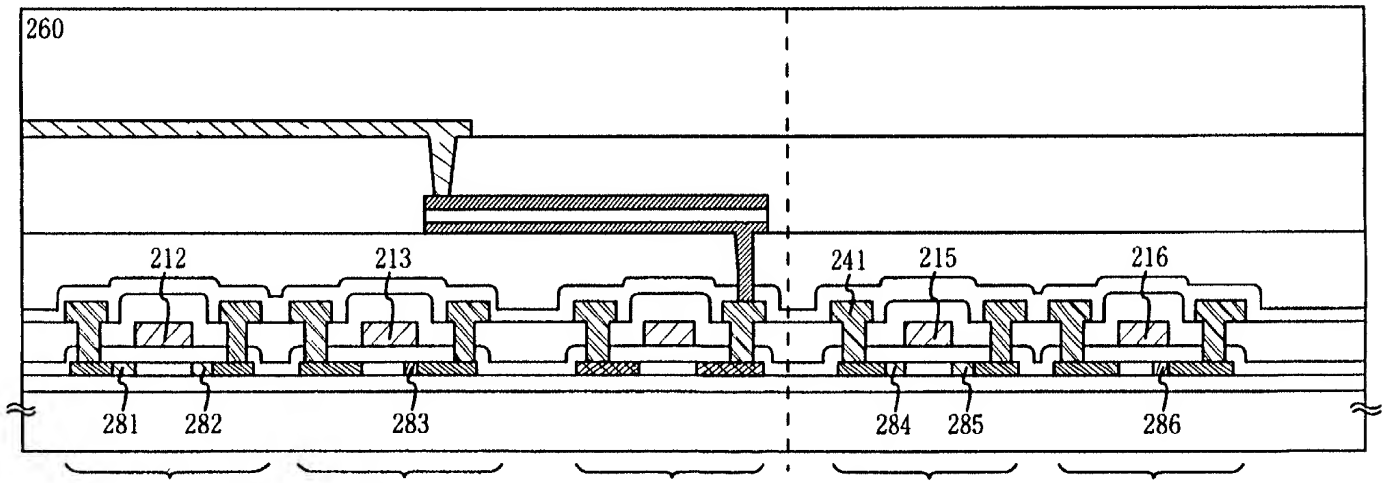


Fig. 33B



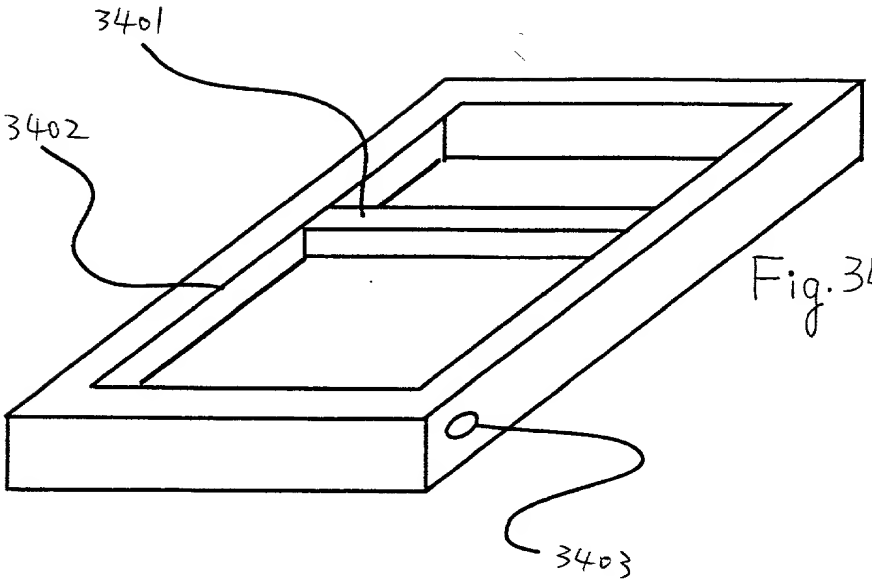


Fig. 34A

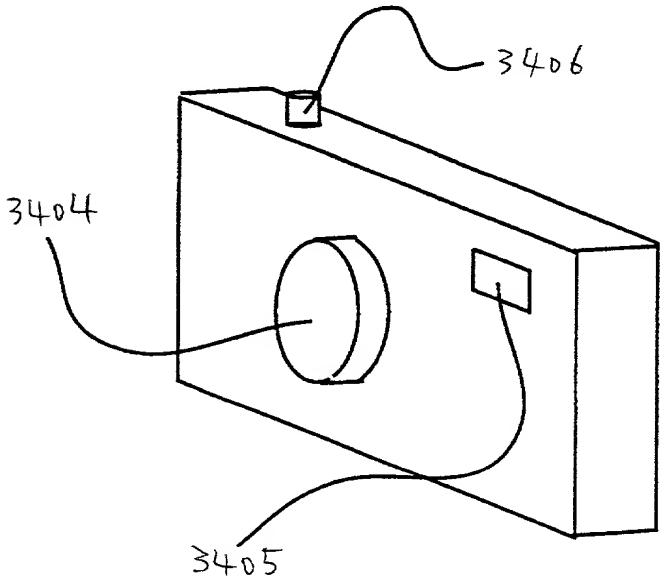


Fig. 34B

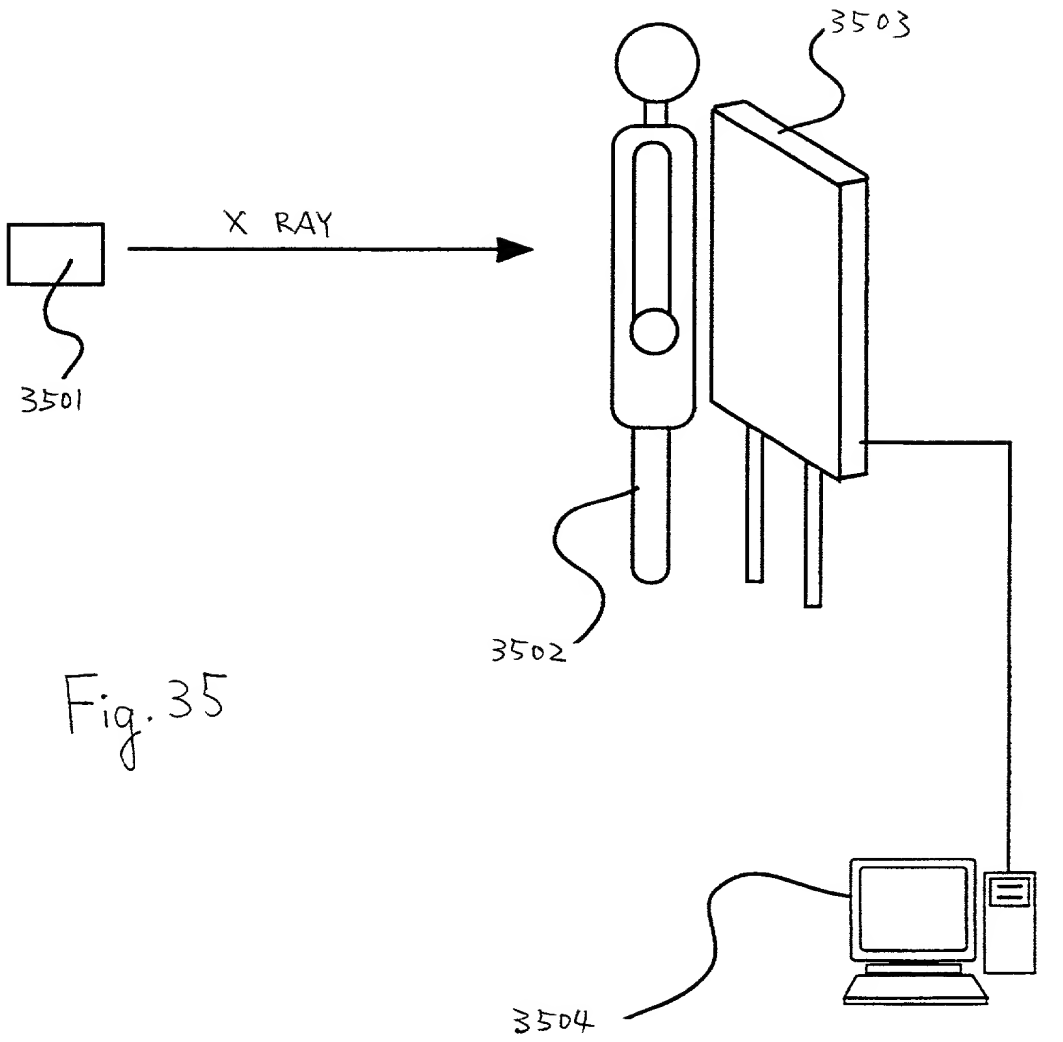


Fig. 35

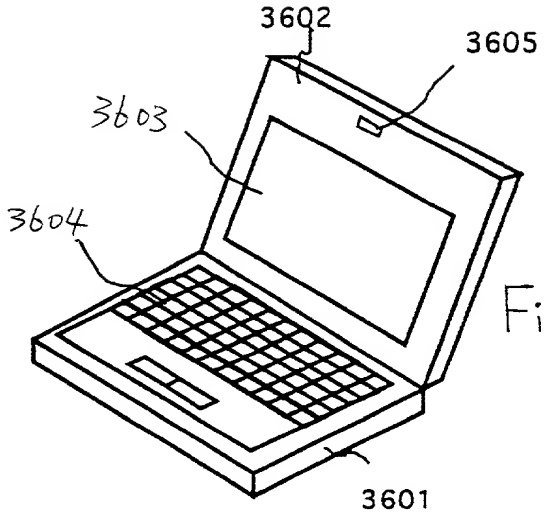


Fig. 36

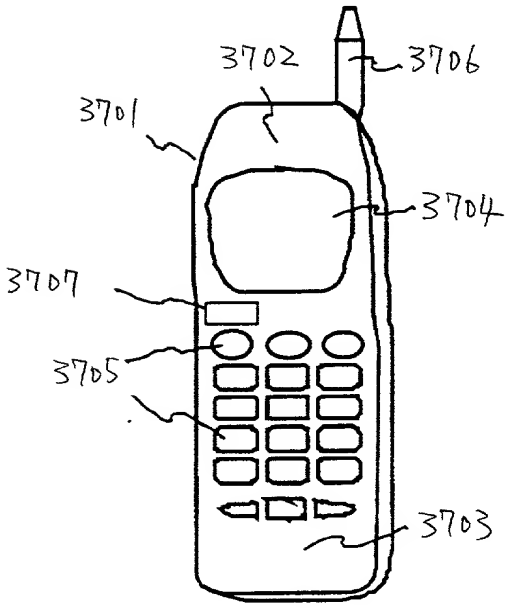


Fig. 37